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L7: Entry 2 of 2 File: USPT Jul 10, 1984

US-PAT-NO: 4459591
DOCUMENT-IDENTIFIER: US 4459591 A

TITLE: Remote-control operating system and method for selectively addressing code-addressable receivers, particularly to execute switching function in automotive vehicles

DATE-ISSUED: July 10, 1984

INVENTOR-INFORMATION:

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FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	3103884	February 5, 1981

INT-CL: [03] H04Q 9/06, H04B 9/00

US-CL-ISSUED: 340/825.57; 340/825.05, 455/603
US-CL-CURRENT: 340/825.57; 398/1, 398/107, 398/111, 398/154

FIELD-OF-SEARCH: 340/825.57, 340/825.05, 340/52F, 340/825.01, 307/1AT, 455/613, 455/606, 455/603, 455/611, 370/4, 370/86

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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☐	4016490	April 1977	Weckenmann et al.	324/61R

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☐	4085403	April 1978	Meier et al.	340/168
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☐	4107555	August 1978	Haas et al.	307/308
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OTHER PUBLICATIONS

"Fast Fiber Bus Points to Fast Local Nets", K. Drefack, Electronics, vol. 53, No. 27, Dec. 18, 1980, pp. 64;66 (S 1628-0074).

ART-UNIT: 234

PRIMARY-EXAMINER: Yusko; Donald J.

ATTY-AGENT-FIRM: Frishauf, Holtz, Goodman & Woodward

ABSTRACT:

To eliminate separate clock, control, and acknowledgment communication lines in a ring-connected remote-control operating system, for example a system applied to a vehicle in which switches (29) or command signals derived from a central station (10) generate code signals to which receivers (11, 12) are responsive to carry out commands, such as energization of a relay (18), a lamp (17), a motor (16, 20) or the like, or cause retransmission to the central station of a sensed operating signal, for example fuel level, for display on a display unit (28), only a single communication line (8), preferably in form of a light guide (15), is provided coupled to the central station (10) and to the respective receivers. The coding is effected by applying to the single line (15) cyclical pulse sequences. The pulse sequences are arranged to form codes which are derived by making the pulses of different pulse widths, and the pulse gaps of respectively different pulse gap widths, and sensing the number of pulses, the pulse widths, and the duration of the pulse gaps between the pulses to thereby obtain coding which is related to clock signals (B), synchronization signals (C), control signals (0, 1), as well as acknowledgment signals (B'). The decoding system includes timing circuits which respond respectively, to the timing pulse pauses and to the time duration of individual pulses.

24 Claims, 6 Drawing figures

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L7: Entry 2 of 2 File: USPT Jul 10, 1984

DOCUMENT-IDENTIFIER: US 4459591 A
TITLE: Remote-control operating system and method for selectively addressing code-addressable receivers, particularly to execute switching function in automotive vehicles

Brief Summary Text (12):
The present invention relates to a remote-control system and method, and more particularly to a method and system for selectively controlling response of receivers to, then, effect, typically, switching or measuring functions. Such a system is useful, for example, in automotive vehicles to control energization of selected loads, for example connection of lights, operation of fans, or other accessories, and further to transmit sensed information, for example available fuel, temperature, or the like. The remotely controlled or transmitting devices are connected for power supply to a power bus and, in accordance with the present invention, to a single control line which provides selective addressing signals as well as acknowledgment signals that the commanded function has been carried out, on the same line.

Brief Summary Text (14):
Various types of remote-control operating and/or sensing or measuring systems are known, and the present invention is specifically directed to the type of system described in the referenced U.S. Pat. No. 4,085,403, MEIER. The system of the referenced patent is specifically arranged to selectively control operation, or sense a measurement value of devices located in automotive vehicles, in which the various devices are spatially distributed throughout the vehicles. For control and transmission of acknowledgment and/or measurement signals, a ring bus system is provided which, for example, can be located within the vehicle and to which receivers are selectively attachable at any location, in which the receivers are supplied with response codes for selective addressing in accordance with the specifically assigned code from operating switches or an operating sequencing circuit. The arrangement is a digital multiplex control system. In accordance with this disclosure, the ring bus system has, besides a power supply bus, a control bus on which, from a central station, clock signals, synchronizing, and control signals are applied, connected to and transmitted to all the receivers associated with all the loads. The respective receivers contain decoding networks so that only that one of the receivers will respond to signals on the lines of the ring bus system which decodes its assigned code on the control bus. The various control signals are applied in cyclical, digital pulse sequence from the central station to the control bus. To report back to the central station that a command applied thereto actually has been executed, an acknowledgment signal is applied to an acknowledgment bus which is part of the ring line or cable. A display, then, indicates that the specific command actually has been executed.

Brief Summary Text (17):
It is an object to simplify the overall system so that the ring bus, to which all the loads are to be connected, will consist only of a single communication line, physically associated, for example, with a power supply cable so that connections to the receiver or subsequently installed receivers can be reliably made to the

single communication line since distinguishing between the power supply bus and the communication line is usually simple.

Brief Summary Text (21):
Utilizing the single communication line in form of a light guide, and transmitting the code in form of light pulses, permits use of a high pulse repetition rate, that is, a high operating frequency, without danger of interfering pulses being applied to the operating line independently of the command system due, for example, to noise pulses which arise in automotive vehicles and which may occur at random. Such noise pulses can be induced in a control bus of an automotive vehicle, for example, when the vehicle passes beneath a high-tension transmission line, adjacent the catenary system of an electric railway, or the like. To prevent erroneous operation, signaling systems utilizing electrical signal transmissions require filtering and/or noise pulse suppression circuits. Using the communication line in form of a light guide avoids the necessity for such additional and accessory apparatus, while improving the signal/noise ratio of the overally system.

Brief Summary Text (23):
Use of the light guide has the specific advantage that it is bilateral, that is, can readily transmit signals between the transmitter and receiver, in both directions, and thus is capable of handling the acknowledgment signals as well as the initial command signals. To couple input and output pulses to the light guide, it is only necessary to couple an electro-optical coupler to the light guide, the electro-optical coupler including, for example, a luminescent diode, or the like.

Detailed Description Text (3):
The light guide 15 has junctions or couplers 21 coupled thereto at all of the receivers, as well as at the central station. The couplers 21 include opto-electrical transducers 22, 23 which are electrically connected with the central station 10 and the receivers 11, 12, respectively. The opto-electrical transducers have a light signal receiver 22, preferably a photo diode, and a light signal transmitter 23, preferably a light emitting diode (LED). The opto-couplers 21, connected to the light guide 15, include at the terminal end thereof a glass window 24 having a mirrored surface 24a, so coupled to the light guide 15 that the plane of the mirrored surface 24a forms an angle with respect to the longitudinal axis X of the light guide 15. The receiver 11 has only a single control output, namely controlling ON/OFF operation of the blower motor 16. For purposes of illustration, the code assigned to the blower motor 16, and hence to the receiver 11, is the count number 1. The receiver 12 actually receives four different codes, for specific association with the four loads 17-20. The loads 17-20 have the count numbers 2, 3, 4 and 5 associated therewith.

Detailed Description Text (4):
The central station 10, which forms a transmitter station, includes a microprocessor or microcomputer 25 which is connected over a data bus 26 to an input unit 27 and to a digitally controlled display or output unit 28. The data input unit 27 has included therein all of the operating switches or operating elements which control operation of the respectively operator-controlled devices, and which have switches 29 associated therewith which are coded to be associated with the respective load devices. In the example, five operating switches 29, and having associated therewith the respective count numbers 1 to 5, are shown, although, of course, many more can be used. Any number of receivers can be coupled to the light guide ring bus 8 to which any number of loads can be connected, for selective control, and which have further count numbers associated therewith, operator-controllable by further switches similar to the switches 29. For example, the left and right headlights of a vehicle may, each, have separate receivers associated therewith, with identical count numbers for the respective codes thereof, so that, upon operation of a single switch of the data input unit 27, both the right and left side headlights will be energized. Different count numbers, of course, will be associated with the right and left side direction blinkers. Since

the receivers 11, 12 are all branched from the single line 8, they are, in effect, in parallel, and also in parallel to the central station 10.

Detailed Description Text (8):
The user, of course, would like to be assured that the particular command which he has entered by the switch 29 of the data input unit 17 actually has been carried out. An acknowledgment signal, thus, is generated in the receiving station 11, 12 to which the respectively addressed load is connected. The acknowledgment to the central station is effected by extending the clock control pulse B to have the duration B'--see FIG. 2, graph f. Acknowledgment can be effected by, for example, an additional relay contact or by placing an additional sensor which senses that the command has been carried out, for example a light sensitive element in light-transmitting relationship to a light bulb which should light upon command in accordance with the specific operation of one of the switches 29.

Detailed Description Text (9):
If the acknowledgment or return signal should transmit a sensed value, for example the level of fuel in a tank, the extent of prolongation of the pulse B' will provide an analog value of the respectively sensed level.

Detailed Description Text (10):
The extent, in time, of the pulse sequence A changes due to the different control signals, as well as due to the different return or acknowledgment signals. Consequently, the length of the pause C (FIG. 2, graph c) will likewise change. The frequency of the pulse sequence A, however, remains invarying or constant.

Detailed Description Text (13):
Example: Let it be assumed that the upper-beam headlights are to be commanded to be used, and that, consequently, switch 29 associated with control number 3 is closed. Data bus 26 supplies the information that number 3 is to be controlled from the data input unit 27 to the microprocessor or microcomputer 25. The microcomputer processes the information in accordance with a simple program such that the central station 10 will provide a cyclical light pulse sequence A (FIG. 2) through the coupler 21 on the light guide 15. The cyclical light pulse sequence, in order to address the device 18 which is associated with control number 3, will have the third clock pulse of the sequence A followed by a longer pause than the other clock pulses, in order to characterize the third pulse as a 1-signal, see graph a of FIG. 2 and graph e. Since the third clock pulse will have a long gap thereafter, the third pulse of the pulse sequence A will address the receiver 12 which has a count number of 3 associated therewith. The receiver includes decoding means which interrogate the pulse sequence A and, upon recognizing the long pause after the third pulse sequence, recognizes, consequently, the 1-signal associated with the number 3. A time delay circuit, which has an adjustable time delay period within the receiver 12 then controls the headlight relay 18 to connect the headlight to ON. The headlight relay has an additional terminal 30 which is a normally closed (NC) terminal, which is used to acknowledge that the command has been recognized and is being carried out. The additional terminal 30 is also connected to the receiver 12--as will appear in connection with FIG. 5--and, as soon as it is open, causes extension of the third clock pulse of subsequent cyclical pulse sequences A by the receiver. This extended clock pulse, the third one since the third address has been addressed, and shown as the extended pulse B', graph f of FIG. 2, is sensed by the central station 10 and, in accordance with the program in the microcomputer 25, a corresponding output is applied to the display unit 28 over the data bus 26, or directly on a suitable indicator lamp on the associated switch 29 of the input unit 27, in accordance with the structural arrangement of the respective input/output and display units which are utilized.

Detailed Description Text (18):
The coupler 21 connected to the light guide 15 has the end of a glass fiber 24 connected to the receiving station 12. The light pulses in light guide 15 are

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transmitted over the fiber 24 to a semi-transparent mirror, located at an end face thereof, for transmission to a pick-up photo diode 35 which, with its anode, is connected to the receiver power bus 13a. The photo diode 35 has its cathode connected to the input of an amplifier 36, the output of which is connected to the count input of a pulse counter 37. The output of the amplifier 36, further, is connected to the input of a reset circuit 38 which includes an inverter 39, and an R/C timing circuit 40 which is connected to a threshold circuit 41. The R/C timing circuit 40 includes a discharge diode 42. The reset or count-erase stage 38 has its output connected to the reset input terminal R of the pulse counter 37. The pulse counter 37, in the example shown, has six output lines 43 from which, as well known, the count state can be determined in binary form. A group of exclusive OR-gates 45 are connected to the count outputs of the counter 37 so that any predetermined count state can be decoded by connecting the second input of the Exclusive OR-gate 44 in accordance with the required decode number to a corresponding positive or negative voltage, available from bus 13a, or ground or chassis connection 46, respectively. The outputs of the Exclusive OR-gates 44 are jointly connected to an AND-gate 45. In the example selected, the pulse counter 37 provides a pulse to the output of the AND-gate 45 when the decimal number 3 appears at the output of the pulse counter 37. To count a binary 11 (decimal 3), the first Exclusive OR-gates 44 are connected with their second to positive bus 13a; the remaining gates 44 have their second input connected to the negative or reference bus 46. The output of the AND-gate 45 is connected over a second AND-gate 47 to the count input of a cycle counter 48 which has two outputs. The cycle counter 48 has both its outputs connected over an AND-gate 49 and through a resistor 50 with an output terminal 51 of the receiving station 12. The load device associated with the receiver and which has the code number 3, in the example selected, the winding of the headlight relay 18, is connected to output terminal 51. In the position shown, the relay is energized and, consequently, the NC terminal 30 for acknowledgement is opened, whereas the normally open (NO) operating contact is closed, so that the head light 53 will be energized and will be lit.

energized
activated

Detailed Description Text (25):
The pulse gaps between clock pulses are sensed both by the reset circuit or stage 38 as well as by the timing circuit 55. The pulse gaps between succeeding clock pulses are much too short to cause the reset circuit to respond. Consequently, the counter 37 is not reset during sequential pulses of the pulse sequence A'. Rather, the capacitor of the R/C circuit 4 will start from discharge state for each pause sequential to a pulse since each pulse causes discharge of the charge which has accumulated on the capacitor of the R/C timing circuit over the discharge diode 42, for grounding the output from the inverter 39 which, then, is connected to ground or chassis. Upon beginning of any pause or pulse gap, a second timing interval is sensed, however, by the timing circuit 55 and the capacitor of the R/C circuit 57 therein will charge gradually--see graph e of FIG. 6. The pulse gap between sequential clock pulses represents a control 0-signal. The timing R/C circuit 57 of the timing stage 55 is so arranged that the output of the timing circuit will have the signal of graph f appear only when the interval between sequential clock pulses is longer, that is, when a control 1-signal is being transmitted. At shorter pulse gaps, the capacitor of the R/C circuit 57 is discharged upon start of the subsequent clock pulses over the discharge diode 59.

Detailed Description Text (30):
The cycle counter 48 insures that the device 18 is not energized by a possible stray pulse applied to, or sensed by the receiving station 12. The cycle counter 48, thus, counts a predetermined number of pulses which are to control operation of the device, in this case energization of relay 18; three such pulses, in three sequential pulse trains or sequences A, are suitable. The device 18 is thus commanded to ON state only if three sequential pulse trains or sequences A provide the appropriate command. The high frequency of the pulse sequence does not cause a delay which can be noticed when controlling a device to be ON or to turn a device OFF.

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Detailed Description Text (32):
(1) Pulses A (FIG. 1) are transmitted from the central station 10.

Detailed Description Text (38):
For synchronization, the central station will also transmit

Detailed Description Text (42):
It is not necessary to use light guides as the transmission conduit; rather than using a light guide 15, a single electrical control line may also be used. Light guides, however, are immune against electromagnetic disturbance fields which, particularly in mobile applications, and especially in motor vehicles, may lead to stray or erroneous pulses. Such disturbance fields and disturbance pulses arise in the on-board vehicular network of automotive vehicles. A remote-control system utilizing a light guide can employ a clock frequency which is substantially higher than that possible with an electrical conductor, so that the number of load devices connected to the ring bus system 8, or the number of sensing stations, can be substantially higher than with electrical conductors, without lowering the operating reliability. The frequency of the pulse train A which, in a preferred example, is in the order of about 20 KHz, may readily be increased. This, of course, then also increases the cycling frequency since the duration of the respective pauses between cycles, that is, the gaps C and C' (FIGS. 2, 6) can be made shorter.

Detailed Description Text (46):
Use of a light guide cable for the control line has the additional advantage that the acknowledgment or other signals can be distinguished from the pulses of the pulse train not only by extended time but, for example, also by color. Thus, it is possible, for example, to provide an LED 66 which has a color output which differs from the LED within the central station 10 which provides the pulses forming the pulse sequence A. By interposition of suitable filters, the photo diode 35 can be made non-responsive to the output from the LED 66; a suitable filter within the coupler 21 between the light guide and the central station 10 then can be utilized for easy separation of pulses from the respective receivers to the central station, and pulses from the central station to the respective receivers. Different colors can also be used to distinguish between basically different receivers, for example colors of one pulse train for receivers which are to be controlled in ON/OFF mode--for example light switches--and receivers which are to transmit data to the central station, for example the level of fuel in the fuel tank. Decoding networks can then be used in the central station or in the receivers, respectively, which may have a code similar to that of other receivers, but which will not be controlled to respond because the respective photoelectric transducers 35, 66 in the receivers, and corresponding photoelectric transducers in the central station reject light for which the particular filters are not transparent, but accept information only if the light in the light guide is appropriate for the particular device or signal which is to be decoded.

CLAIMS:

1. Method of remotely controlling operation of a remote-control operating system for selective addressing and control of one of a plurality of receivers (11, 12) from a central station (10),

particularly to selectively address and control operation of accessory apparatus or devices (16, 17-20) in a motor vehicle, having

a data input unit (27, 25),

including operating switches (29) associated with respective apparatus or devices to address the respective apparatus or devices;

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a data receiver and display unit (28) to display the state of an addressed apparatus or device;

a ring bus (X, 15), all the respective receivers associated with respective apparatus or devices being connected to said ring bus;

code generating and recognition means (10, 10a) connected to the data input unit and to the ring bus, and hence to the receivers, for generating codes representative of one of the receivers, of a function thereof, and decoding data transmitted by the receivers indicative of execution of a decoded operation or command;

and decoding means (37, 44, 45, 38, 55) and code generating means (64) included in the receivers, responding to a characteristic pulse arrangement representative of a code assigned to the respective receivers,

comprising

connecting the ring bus as a closed loop single communication line (X, 15) and connecting said code generating and recognition means (10, 10a) and all the receivers (11, 12) in parallel to the ring bus;

generating, in the code generation and recognition means, cyclically recurring binary pulse sequences which comprise clock (B) and synchronizing signals (C), and data or control signals (A, 0, 1);

generating in the receiver acknowledgment code signals (B'),

wherein said signal generating steps comprise

coding said cyclically recurring binary pulse sequences by generating

(1) a synchronizing and clock signal combination which comprises a first pulse (B) and a subsequent pulse gap having a first and long time duration (C, C');

(2) data or control signals which comprise

(i) pulses (A, A') (1, 2, 3 . . .) of a first predetermined pulse length to denote pulses being transmitted in a first direction between the code generating and recognition means and one of said receivers, and

(ii) pulse gaps (a) between said pulses which have two different second and third gap lengths in dependence on whether the pulse gaps are representative of a binary ZERO or a binary ONE,

both said pulse gaps being short with respect to said first long time duration, and

(iii) pulses (B') of a second predetermined pulse length to denote pulses being transmitted in reverse direction between the code generating and recognition means and one of said receivers;

and transmitting all said coded signal pulses with the respective pulse lengths and pulse gaps between the transmitter and receiver over said closed loop single communication line (X, 15) and forming said ring bus.

5. Method according to claim 4, wherein the step of generating an acknowledgment signal comprises changing the pulse width from that determined by a reference (clock B) by extending the width of one of the pulses of the pulse sequence to

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thereby place on the ring bus (X, 15) a signal which is modified by the receiver with respect to the signal which is transmitted by the code generation and recognition means, the extended pulse being recognized in the code generating and recognition means (10, 10a) for actuation of the data receiver and display unit (28).

6. Method according to claim 1, further comprising the step of counting cycles of binary pulse sequences including said synchronization and clock signal combination and the data or control signals comprising pulses (A, A') (1, 2, 3 . . .) of a first predetermined pulse length and pulse gaps (a) between said pulses of one of said predetermined second and third gap lengths; and

if the particular decoded number within the binary pulse sequence and associated with a specific receiver, as determined by the specific count decoding stage, has been decoded to determine that the same receiver is to be addressed by the same code being transmitted, in succession, a number of times in accordance with a predetermined count number, then and only then generating said pulses (B') of said second predetermined pulse length;

and only then controlling operation of the respective apparatus or device addressed in accordance with the code representative of the receiver associated with the selected apparatus or device.

7. Remote-control operating system for selectively addressing and controlling one of a plurality of receivers (11, 12), particularly for selective addressing and control of operation of accessory apparatus or devices (16, 17, 18, 19, 20) of a motor vehicle having

a data input unit (27, 25) including operating switches (29) associated with respective apparatus or devices;

a data receiver and display unit (28) to display the state of addressed apparatus or devices with which the receiver is associated;

a ring bus (X, 15) to which all the receivers are connected;

code generation and recognition means (10, 10a) connected to the data input unit (27), the data receiver and display unit (28) and to the ring bus (8, 15), and hence to the receivers (11, 12), for generating codes representative of one of the receivers, or of a function of one of the receivers, and decoding data re-transmitted by the receivers indicative of execution of a decoded operating command;

and decoding means (37, 45, 38, 55) included in the receivers responding to a pulse arrangement representative of a code appearing on the ring bus (8, 15),

wherein

the ring bus comprises a closed loop single communication line X, 15;

said code generating and recognition means (10, 10a) and all said receivers (11, 12) being connected in parallel to the ring bus;

the code generation and recognition means generate a digital binary pulse code, coupled to the ring bus, which comprises cyclically recurring binary pulse sequences which include clock (B) and synchronizing signals (C), and data or control signals (A, 0, 1);

the code generation and recognition means (10, 10a) comprises

(1) means for generating a synchronizing (B) and clock (C) signal, in which said synchronizing and clock signal comprises a first pulse (B) and a subsequent pulse gap having a first and long time duration (C, C'); and

(2) means for generating data or control signals which comprise

(i) pulses (A, A'; 1, 2, 3 . . .) of a first predetermined pulse length to denote pulses being transmitted in a first direction between the code generating and recognition means (10, 10a) and all said receivers (11, 12), and

(ii) pulse gaps (a) between said pulses which have two different second and third lengths, in dependence on whether the pulse gaps are to represent a binary ZERO or a binary ONE,

both said pulse gaps being short with respect to said first long time duration;

the receivers include, each, code generating means (64) generating acknowledgment signals (B'),

said acknowledgment signals comprising pulses of a second predetermined pulse length, to denote pulses being transmitted in reverse direction between the pulse generating and recognition means and one of said receivers;

the closed loop single communication line (X, 15) carrying all the signals with the respective coding distinctions for addressing being represented by respective widths of pulses and gaps between pulses.

8. System according to claim 7, wherein said single communication line comprises a light guide (15) carrying said recurring pulse sequences (A) in the form of light pulse sequences being transmitted between the code generation and recognition means (10, 10a) and all of said receivers (11, 12, 12a).

10. System according to claim 9, wherein the opto-electrical transducers at said branching and coupling stations (21) include optical-electrical receivers (23, 35) to receive light signals coursing in the light guide, and opto-electrical transmitters (22, 66) to transmit light pulses in accordance with applied electrical signals into the light guide for coursing in the form of light pulses therein.

17. System according to claim 14, further including a pulse sequence cycle counter (48) connected between the output of the count decoding stage (44, 45) decoding the outputs from the pulse counter (37) and said operating circuit means (50, 51), said cycle counter providing an output to the operating circuit means if, and only if, the particular decoded number associated with the specific receiver as determined by the specific count decoding stage has determined that the same receiver is to be addressed by the same code being transmitted, in succession, a number of times in accordance with the count number of the cycle counter.

18. System according to claim 16, further including a pulse sequence cycle counter (48) connected between the output of the count decoding stage (44, 45) decoding the outputs from the pulse counter (37) and said operating circuit means (50, 51), said cycle counter providing an output to the operating circuit means if, and only if, the particular decoded number associated with the specific receiver as determined by the specific count decoding stage has determined that the same receiver is to be addressed by the same code being transmitted, in succession, a number of times in accordance with the count number of the cycle counter;

and wherein the cycle counter is connected to and controlled by the output from the conjunctive gate (47).

21. System according to claim 7, wherein the means for generating the pulses of a second predetermined pulse length in the receiver includes acknowledgment circuit means (30) providing an acknowledgment output signal representative of response of the device or apparatus in accordance with an addressed command transmitted from said data input unit through the code generating means;

an acknowledgment timing means (64), the output of said acknowledgment timing means being connected to provide an extension signal to said single communication line forming the ring bus,

said acknowledgment timing means being connected to and controlled by operation of a device to provide a timing pulse when the decoding means in the receiver recognizes the presence of a particular pulse in said cyclically recurring pulse sequence and associated with a specific receiver, to thereby extend the length of said pulse coursing in the ring bus and permit recognition of the extended pulse by the code generation and recognition means (10, 10a) in the central station, and thus permit display by the data receiver and display unit (28) that the addressed apparatus or device has received the addressing command.

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L10: Entry 5 of 22 File: USPT Jan 6, 2004

US-PAT-NO: 6672151
DOCUMENT-IDENTIFIER: US 6672151 B1

TITLE: Apparatus and method for remote sensing and receiving

DATE-ISSUED: January 6, 2004

INVENTOR-INFORMATION:

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Campbell; Alan J.	New Berlin	WI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sentech, Inc.	Appleton	WI			02

APPL-NO: 10/ 051967 [PALM]
DATE FILED: January 15, 2002

PARENT-CASE:
RELATED PATENT APPLICATIONS This is a continuation of and claims the benefit of the priority date of U.S. application Ser. No. 09/042,226, filed on Mar. 13, 1998; now U.S. Pat. No. 6,357,292 which is a continuation of application Ser. No. 08/530,938 filed on Sep. 20, 1995, now issued U.S. Pat. No. 5,728,933; which is a divisional of application Ser. No. 08/226,664 filed on Apr. 11, 1994, now issued U.S. Pat. No. 5,483,826; which is a continuation of application Ser. No. 07/792,134 filed on Nov. 13, 1991, now issued U.S. Pat. No. 5,301,553; which is a continuation-in-part of application Ser. No. 07/453,785 filed on Dec. 20, 1989, now issued U.S. Pat. No. 5,083,457. The disclosure of application Ser. No. 09/042,226, titled "Apparatus and Method for Remote Sensing and Receiving", and filed on Mar. 13, 1998 is incorporated by reference herein.

INT-CL: [07] G01 L 9/00, B60 C 23/02

US-CL-ISSUED: 73/146.5
US-CL-CURRENT: 73/146.5

FIELD-OF-SEARCH: 73/146.5, 73/146.8, 73/118.1, 73/178R, 73/706, 73/715-727, 73/714, 73/753, 73/756, 340/442-448

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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ART-UNIT: 2855

PRIMARY-EXAMINER: Oen; William

ABSTRACT:

A sensing and displaying system is provided including a sensor unit having a transducer disposed in intimate contact with a vessel. The transducer senses a characteristic within the vessel like pressure and outputs an electrical signal representative thereof. The sensor unit further includes a response signal generator which transmits a signal representative of the characteristic. A receiver unit receives the transmitted signal and converts it to visual indicia of the characteristic, for example, a number on a liquid crystal display. The system is capable of two-way communication between the sensor unit and the receiver unit. Both the sensor unit and receiver unit store transmitted data in internal memory.

19 Claims, 28 Drawing figures

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DOCUMENT-IDENTIFIER: US 6672151 B1
TITLE: Apparatus and method for remote sensing and receiving

Abstract Text (1):
A sensing and displaying system is provided including a sensor unit having a transducer disposed in intimate contact with a vessel. The transducer senses a characteristic within the vessel like pressure and outputs an electrical signal representative thereof. The sensor unit further includes a response signal generator which transmits a signal representative of the characteristic. A receiver unit receives the transmitted signal and converts it to visual indicia of the characteristic, for example, a number on a liquid crystal display. The system is capable of two-way communication between the sensor unit and the receiver unit. Both the sensor unit and receiver unit store transmitted data in internal memory.

Brief Summary Text (2):
The present invention relates, generally, to a transmitter and receiver combination for measuring a parameter, pressure, force, or weight, within a vessel, and more particularly, to a sensor unit including a transducer and an infrared generator cooperating therewith, for transmitting infrared signals to a remote receiver unit including a measurement display.

Brief Summary Text (10):
The present invention provides a remote sensing and receiving system including a sensor unit and a remote receiver unit. The sensor unit includes a transducer disposed to sense the physical parameter of an apparatus. The transducer generates an electric signal representative of the magnitude of the physical parameter and applies this signal to an LED driver. The LED driver modulates an LED, which transmits an infrared (IR) signal.

Brief Summary Text (12):
The present invention also can be configured to allow for two-way communication between the sensor unit and remote receiver unit. The receiver unit controls the sensor unit by transmitting activation signals for turning the sensor unit on, reading signals for requesting data from the sensor unit, and writing signals for transmitting data to the sensor unit. The sensor and the receiver unit each have a transmitter and a receiver to enable communication through pulses of carrier signals. The data communicated can be stored in memory in the sensor unit or the receiver unit.

Drawing Description Text (3):
FIG. 1 is a schematic representation of a remote display unit and a transmitter unit, including a transducer mounted on a conventional vehicle tire;

Drawing Description Text (11):
FIGS. 12 and 13, are representations of communication signals transmitted and received by the sensor unit and receiver unit;

Detailed Description Text (5):
Pressure sensor unit 16 is advantageously configured to sense tire pressure,

generate an electrical signal indicative of the sensed pressure, and apply the signal to signal converter 34. signal converter 34 converts the pressure signal into an encoded form suitable for use as a modulating signal for LED 38, i.e., LED 38 is modulated in a manner which represents the sensed pressure as a selected characteristic of the encoded signal, e.g., frequency, pulse code, pulse width, etc. Signal converter 34 includes a suitable encoder, such as, for example, a voltage-to-frequency converter, an analog-to-digital converter, a voltage-to-pulse width converter, or the like, and supporting circuitry.

Detailed Description Text (7):
Referring now to FIG. 2B, display unit 12 includes: a battery circuit 41; an appropriate sensor 42, e.g. an IR sensor; a processor 44; and a conventional display 46. The modulated signal transmitted by LED 38 is received at display unit 12 by sensor 42. The voltage from battery 41 is applied to sensor 42, and is modulated in accordance with the response signal received from transducer circuit 14. The modulated signal is applied to a processor 44, wherein information is extracted from the signal and manipulated into a form suitable for application to display 46. Display 46 generates visual indicia, for example a digital readout, representative of tire pressure. A specific embodiment of display unit 12 will hereinafter be described in more detail in conjunction with FIGS. 3 and 4.

Detailed Description Text (8):
As discussed in greater detail below, the functions performed by the various elements comprising the foregoing schematic circuit diagrams may be implemented in a variety of ways. For example, the functions performed by transducer unit 14 may be embodied in a unitary microchip (integrated circuit) for convenient disposition within the valve stem or valve stem cap of a vehicle tire. The functional elements comprising the display unit 12 may similarly be implemented in a microchip or microprocessor, and incorporated into a hand-held remote control display device.

Detailed Description Text (15):
In response to the application of the pulsed command reference signal to the base of transistor Q2, VCC is applied across respective LEDs D2, D3 and D4. Respective LEDs D2-D4 suitably comprise respective IR emitters, Model No. LD271, manufactured by Seimens-Litronix. Thus, respective LEDs D2.varies.D4, under the control of processor U3, generate emissions modulated with a predetermined frequency (tone). As described in greater detail below, the frequency modulated infrared signal transmitted by command generator 56 comprises a "wake-up" command signal C5 used to activate transducer unit 14. Also as described in greater detail below, transducer unit 14 responsively transmits an infrared signal, indicative of tire pressure, back to display unit 12.

Detailed Description Text (22):
In a preferred embodiment of the present invention, transducer unit 14 is configured for disposition within a modified valve stem cap for use in conjunction with conventional vehicle tire valve stems (see FIG. 9). In this manner, a low cost pressure sensor circuit may be powered by a battery which, upon depletion of power, may be discarded. Nonetheless, it is desirable to construct the transducer circuit such that a minimum amount of power is consumed. Transducer unit 14 therefore preferably operates in alternative "dormant" and "active" states. The active state is triggered by reception of command signal CS from display unit 12.

Detailed Description Text (29):
Transducer 60 suitably comprises an electromechanical transducer capable of generating a low level voltage output, for example between 0 and 10 volts, in response to the application of pressures in the range typically exhibited by vehicle tires, i.e., up to 150 psi. Piezoelectric materials are known to be excellent transducers. Although it is desirable to miniaturize the pressure sensing circuit in the preferred embodiment, a pressure sensor Model No. 24 OPC manufactured by Microswitch has yielded satisfactory results in the laboratory.

Those skilled in the art will appreciate that transducer 60 may comprise a suitable microsensor.

Detailed Description Text (44):
If processor U3 determines that switch S is depressed, the output at pin 39 is enabled, thereby applying the command reference signal to command generator circuit 56 and transmitting command signal CS to transducer circuit 52 (step 110).

Detailed Description Text (67):
Pressure transducer 60 (not shown in FIG. 9) is suitably housed within housing 172. signal conversion circuitry, such as that described in connection with signal convertor 34 (FIG. 2), is also housed within housing 172. Similarly, the transmitter and transmitter driver components, analogous to LED 38 and LED driver 36 of FIG. 2, may be housed within housing 172. Alternatively, IR unit 168 may perform the dual function of receiving a command signal and transmitting a response signal, in which case sensor 168 may also comprise an appropriate LED (not shown). In yet a further alternate embodiment, the response generator (LED and driver) may be disposed proximate an opening which extends through the side of cap 124 proximate housing. 172.

Detailed Description Text (71):
Sensor unit 400 is affixed to fire extinguisher device 305 preferably near the nozzle 307. A transducer 422 is disposed within the pressurized tank of fire extinguisher 305. Sensor unit 400 is attached in or on fire extinguisher device 305 so that sensor unit 400 can transmit signals via an infrared output 460. Those skilled in the art will appreciate that sensor unit 400 may be mounted in various places so that transducer 422 is exposed to the pressure in the tank of fire extinguisher 305 and infrared output 460 is exposed to the exterior of extinguisher 305.

Detailed Description Text (73):
Sensor unit 400 and a receiver unit 500 are employed in the inspection and maintenance of fire extinguisher devices. In order for proper inspection, sensor unit 400 must be capable of transmitting data to receiver unit 500 indicative of the identification of the fire extinguisher. By way of example, identification data may include an identification number, a filling sight number, the date and time of inspection, and status of the fire extinguisher. Some of this data can be input into a memory 434 at the time fire extinguisher 305 is filled or at the time sensor unit 400 is provided at fire extinguisher 305. This data can also be programmed into memory 434 by receiver unit 500. If memory 434 is powered memory, switch 453 must be closed before loading any data into memory.

Detailed Description Text (77):
In the normal course of building maintenance, an inspector holding receiver unit 500 periodically walks up to fire extinguisher device 305 employed with sensor unit 400. The inspector presses the appropriate keys on a keyboard 526 in order to activate sensor unit 400. In response to the appropriate keys and or switches, receiver unit 500 transmits an activation signal to sensor unit 400. An activation is a signal like a start-up signal which turns on a particular device. In response to this activation signal, sensor unit 400 is turned "ON" and transmits signals indicative of characteristics of fire extinguisher device 305 and sensor unit 400.

Detailed Description Text (79):
Referring now to FIG. 10, sensor unit 400 includes an activation circuit 440, a pressure measurement circuitry 420, a processor circuitry 430, infrared output 460 and battery 410. Activation circuit 440 includes an infrared detector circuit 441, a power switch circuit 450 and a power source transistor 454. Infrared detector circuit 441 includes an infrared sensor 442, a gain amplifier 444, a band pass filter 446, and a detector circuit 448. As is well known in the art, most circuit elements on sensor unit 400 could be reduced and combined with other elements onto

a single microchip. This reduction saves manufacturing time, power requirements, and size.

Detailed Description Text (80):
The interaction the circuits in FIG. 10 are explained generally as follows. Detector circuit 441 detects infrared signals and generates demodulated electric signals. These signals are provided to processor circuitry 430, pressure measurement circuitry 420, and activation circuit 440.

Detailed Description Text (84):
The circuitry in sensor unit 400 generally is in a dormant state until turned "ON" by activation circuit 440. Sensor unit 400 saves energy from battery 410 by operating in the "STANDBY" mode unless communicating with receiver unit 500. In the "STANDBY" mode, all circuitry in sensor 400 is powered down except for infrared detector circuit 441, activation circuit 440, and memory 434. Activation circuit 440 turns remote sensor unit 400 "ON" when activation circuit 440 receives the proper signal from receiver unit 500. In the preferred embodiment the proper signal is 19 kHz carrier signal although sensor unit 400 could be configured for various frequencies. Sensor unit 400 is in a "STANDBY" mode at all other times.

Detailed Description Text (85):
When an activation signal from receiver unit 500 is transmitted to remote sensor unit 400, activation circuit 440 provides a path to power for other circuit elements. Power source transistor 454 is turned on to provide the path to battery 410. The circuit elements that receive power through transistor 454 are processor circuitry 430, pressure measurement circuit 420, and infrared output 460.

Detailed Description Text (87):
The encoded signal indicative of pressure produced by processor circuitry 430 is applied to infrared output circuit 460. An infrared LED 465 is modulated in a manner which represents the sensed pressure as a selected characteristic of the encoded signal, e.g., frequency, pulse code, pulse width, etc. In a preferred embodiment, infrared output circuit 460 drives infrared LED 465, which emits a modulated pulse response signal, suitably in the infrared frequency range, indicative of pressure. The LED emissions are preferably directional so that the inspector can determine which sensor unit 400 is being read by the relative position of receiver unit 500 to sensor unit 400.

Detailed Description Text (88):
Referring now to FIG. 11, receiver unit 500 suitably comprises: a power circuit 510, a computer circuit 520, and a transmitter circuit 540. Power circuit 510 includes a battery 512, a switch 514, and a voltage regulator 516. Switch 514 is a standard user activated switch for turning "ON" the receiver unit 500. Receiver unit also includes a receiver circuit 580.

Detailed Description Text (90):
Computer circuit 520 also is responsible for creating control signals such as read, write, and activations signals. These signals are generated by computer circuit 520 in response to commands form the user or software. These signals are provided to transmitter 540. Transmitter 540 modulates these signals and produces a modulated infrared signal for sensor unit 400.

Detailed Description Text (91):
Receiver unit 500 is advantageously configured to transmit control signals like activation signals, read signals, and write signals. Activation signals cause activation circuit 440 to turn "ON" components in sensor unit 400; read signals cause processor circuitry 430 to initiate generation of signals indicative pressure data or other data by sensor unit 400; write signals cause data transmitted by receiver unit 500 to be stored in memory 434 of sensor unit 400. Computer circuit 520 creates these signals which are transmitted to sensor unit 400. These signals

are initiated by a program stored in memory 522 or from user manipulation of keyboard 526 or other switches.

Detailed Description Text (92):
Computer circuit 520 applies these control or processor signals to transmitter circuit 540. Transmitter circuit 540 modulates an infrared LED 548 in accordance with processor signals or signals initiated by computer circuit 520. Receiver unit 500 communicates processor signals to sensor unit 400 by modulating LED 548 in a particular frequency, pulse code, pulse width, etc. Preferably, infrared LED 548 operates in the infrared frequency range.

Detailed Description Text (98):
A description of the preferred internal operation of the remote sensing and receiving system is described as follows with reference to FIGS. 10, 11, 12 and 13. With switch 514 closed, the operator can initiate an activation signal 610 through keyboard 526 or a program stored in memory 522 or micro & peripheral circuit 524. Activation signal 610 is transmitted as pulses of particular frequency or tone as in signal 612; in a preferred embodiment pulses of a 19 kHz signal provides an activation signal 610. Micro & peripheral circuit 524 creates an activation signal when micro & peripheral circuit 524 enables transmitter circuit 540. Processor circuitry changes the state of an input 541 of the AND gate 544 to a logic high. An input 543 of AND gate 544 is a 19 kHz carrier signal created by an oscillator 542. When input 541 is high, the output of AND gate 544 is the same signal received by input 543; in this embodiment, a 19 kHz carrier signal is transmitted as long as input 541 is high. This signal travels across a resistor 545 and turns a transistor 546 on and off at a frequency of 19 kHz. As transistor 546 is modulated at 19 kHz, a 19 kHz signal travels through infrared LED 548 and a resistor 547. Infrared LED 548 produces an infrared signal modulated at 19 kHz in response to the electrical signal. In other words, a 19 kHz carrier signal of infrared light is produced by infrared LED 548 and transmitted to sensor unit 400.

Detailed Description Text (99):
With reference to FIG. 13, a signal 612, a 19 kHz carrier signal, is demodulated as a signal 614, an ON signal. An activation signal is shown as activation signal 610 or as part of hand-held read signal 620.

Detailed Description Text (100):
When any infrared light is transmitted to sensor unit 400, infrared sensor 442 produces an electric signal proportional to the amount of infrared light received. The electric signal is amplified by gain amplifier 444 and input into band pass filter 446. Band pass filter 446 filters signal eliminating any signals not of the proper frequency. Preferably, band pass filter 446 is tuned so that only 19 kHz signals are transmitted to detector 448. Detector 448 receives the filtered signal and demodulates the 19 kHz carrier signal into clock pulses representing the presence of the carrier signal as represented by signal 612. In other words, detector 448 preferably generates a pulse signal similar to the pulse signal created by micro & peripheral circuit 524 and transmitted to input 541. Detector 448 transmits this pulse signal to power switch circuit 450, pressure measurement circuit 420, and processor circuitry 430. Communications between sensor unit 400 and receiver unit 500 are explained as follows from the perspective of the receiver unit 500.

Detailed Description Text (101):
Power switch circuit 450 turns power source transistor 454 to an "ON" state in response to an activation signal. Power switch circuit 450 keeps power source transistor 454 "ON" for a specific amount of time after a signal. Power source transistor 454 provides a path to power other circuit elements in sensor unit 400. The activation signal must be at least 2 pulses in order to keep the sensor unit 400 in an "ON" mode. The activation signal is chosen as two pulses rather. than one in order to ensure the reliability of signal reception. In the preferred

embodiment, logic circuits and counters are used as part of power switch circuit 450 to turn sensor unit 400 "ON" after receiving the two pulses of activation signal 610. The device can be configured to have various activation signals. For example, a less conservative approach could simply use one pulse to activate sensor unit 400. An activation signal is a necessary part of both read and write signals as is explained below.

Detailed Description Text (102):
Computer circuit 520 creates read signals so that sensor unit 400 transmits data to receiver unit 500. With reference to FIG. 13, read signal 620 is produced by receiver unit 500 upon initiation by operator or program stored in memory 522. The first part of read signal 620 is an activation signal. The rest of read signal 620 are clock pulses which initiate the transmission of data by sensor unit 400.

Detailed Description Text (103):
Read signal 620 is created in the transmitter circuit 540 similarly to activation signal 610. Micro & peripheral circuit 524 sends pulse signals to the input 541 of AND gate 544. In response to this signal, LED 548 is modulated to produce pulses of 19 kHz carrier signals.

Detailed Description Text (104):
In response to this first activation signal, sensor unit 400 is turned "ON". When sensor unit 400 is turned ON from the dormant state or "STANDBY" mode, the sensor unit begins in read mode, state 1. After the activation signal, receiver unit 500 sends clock pulses of 19 kHz carrier signal; these pulses are part of read signal 620.

Detailed Description Text (105):
In the read mode, state 1, sensor unit 400 determines the pressure and transmits pressure data back to receiver unit 500 synchronously with the clock pulses of read signal 620. The pressure data is transmitted in the form of a sensor read signal 624. Once micro & peripheral circuit 524 receives a pulse representing data in sensor read signal 624, receiver unit 500 transmits another pulse. In response to this pulse, sensor unit 400 transmits another pulse representing data. Sensor unit 400 and receiver unit 500 repeat these operations until the requested data is transmitted by sensor unit 400.

Detailed Description Text (106):
After the data is received, processing circuitry 524 evaluates the pressure data from sensor 400, and then turns input 541 of AND gate 544 low so that receiver unit 500 ceases the transmission of the 19 kHz carrier signal. Sensor unit 400 is deactivated because of this absence of signals.

Detailed Description Text (107):
After deactivation, receiver unit 500 repeats this read sequence with the read signal 622 in order to verify the first reading. If the pressure data received by receiver unit 500 is the same as the first reading, the pressure data is converted into a readable form and displayed on LCD display 532 or stored in memory 522. If the pressure data is different than the first reading, receiver 500 repeats the procedure with another read signal 620. The pressure data is preferably displayed on LCD display 532 in pounds per square inch.

Detailed Description Text (108):
When additional information is desired from the sensor unit 400, receiver unit 500 transmits read signals so that sensor unit 400 operates in a different state. Receiver unit 500 changes the state of sensor unit 400 by holding the carrier signals "ON" for a specific length of time without pulses. If the carrier signal is off for a specified length of time, sensor unit 400 will be deactivated; upon start-up, sensor unit 400 begins in the read mode, state 1 again.

Detailed Description Text (110):
After the carrier "ON" signal has been sent for an appropriate length of time, receiver unit 500 transmits an activation signal of at least two pulses so that sensor unit 400 changes states. Sensor unit 400 changes states in response to this activation signal and the pulse signal from charge circuit 431. In the new state, sensor unit 400 transmits new information corresponding to the different state in response to clock pulses from the receiver unit 500.

Detailed Description Text (111):
With reference to FIG. 13, a read signal 630 activates sensor unit 400 "ON" and transmits the carrier signal until state 2 is reached. When state 2 is reached, receiver unit 500 transmits another activation signal followed by the carrier signal to reach state X. When state 2 is surpassed, receiver unit 500 transmits another activation signal followed by clock pulses so that sensor unit 400 transmits data in state X.

Detailed Description Text (112):
In response to the clock pulses, sensor unit 400 synchronously transmits pulses representing information as shown in read signal 630 and the a sensor read signal 632. These clock pulses allow the receiver unit 500 to keep track of the information received. With this method, information is not received out of sequence because each bit of data is transmitted upon initiation of a clock pulse from receiver unit 500. Receiver unit 500 does not send another clock pulse until the requested bit is received. After all the bits making up the requested data are received, receiver unit 500 does not send any more clock pulses.

Detailed Description Text (113):
As an example, when the sensor unit 400 is in the read mode, state X, identification data is transmitted to receiver unit 500. Sensor unit 400 stores the identification data in memory 434. The data is transmitted serially from memory 434 to multiplexer 432. In a particular embodiment, memory 434 includes a shift register for outputting data. State counter 435 addresses the memory location associated with a given state so that memory 435 outputs the data to the shift register. The clock pulses in read signal 630 initiate a serial output of the data one bit at a time by the shift register.

Detailed Description Text (114):
Various states could be reached by sensor unit 400 through the method of activation signals and carrier signals described above. In these various states, various information could be sought and transmitted according to the users needs.

Detailed Description Text (115):
State X is not the limit of states; other states can be reached by the same technique. For instance, activation signals and carrier signals can be transmitted at appropriate times in order to reach read mode, state Y. In state Y, sensor unit 400 synchronously transmits different information in response to pulses transmitted by receiver unit 500. This different information could be stored in a memory location in memory 434 which is addressable by state counter 435. For example, this different information could be the date of the last measurement of pressure. This procedure can be continued in this fashion until all desired information is obtained.

Detailed Description Text (116):
With reference to FIG. 13, read signal 630 shows that different states can be reached without having to transmit data at every previous state. This feature saves energy as LED 465 is not driven unnecessarily. For instance, read signal 630 reaches state X without having sensor unit 400 transmit data in states 1 and 2. Read signal 630 skipped the data in states 1 and 2 by not providing any clock pulses in between activation signals, instead a constant carrier signal was provided. In contrast, read signal 620 provided for the reception of the data of

state 1 by transmitting clock pulses after the activation signal.

Detailed Description Text (117):
The write mode is slightly more complicated than the read mode. Unlike the read mode, receiver unit 500 must send specific data to sensor unit 400 in the write sequence. The data is represented by a series of pulses. This data can be location data, identification data, barometric pressure, the date, or any other data for use or storage by sensor unit 400. The series of pulses are generated by processing circuitry 524 and sent through transmitter circuit 540.

Detailed Description Text (118):
With reference to FIG.12, the write mode is reached in sensor unit 400 with activation signals and providing change state signals with carrier signals for a specified amount of time. Preferably, the write mode is after the last state in the read mode. In other words, receiver unit 500 transmits a series of activation signals followed by carrier signals for a specified length of time until all read states have been surpassed. Once the write mode and proper state is reached, receiver unit 500 sends data corresponding to the state.

Detailed Description Text (119):
Just as the correct state had to be reached in the read mode, the correct state has to be reached for the write mode. For instance, if the operator is transmitting identification data to sensor unit 400, sensor unit 400 should be in the write mode, state X where state X is the state for receiving the first number of the identification.

Detailed Description Text (120):
For example, in order to store identification number 00225, there are five identification states, one for each digit. After the write mode is reached, sensor unit 400 is put in state X by transmitting the write signal 640. Write signal 640 is a combination of an activation signal and carrier signals. After the appropriate mode is reached, the first digit is input by transmitting an activation signal (two clock pulses) and the digit (5 clock pulses). Again, two clock pulses for an activation signal are not required; the circuit can be designed so that one would be sufficient. However, two clock pulses are implemented in this design because two pulses are more reliable. In other words once correct state is reached, receiver unit 500 transmits seven clock pulses. Upon receiving the activation signals, sensor unit 400 synchronously transmits the data back to receiver unit 500 as in the sensor write signal 650. Receiver unit 500 verifies that the data transfer was correct. If the data received was not correct, receiver unit 500 does not advance sensor unit 400 into the next state, and transfers the data again.

Detailed Description Text (121):
In response to the data represented by clock pulses, sensor unit 400 stores the digit five in memory 434 in a space reserved for the first identification number. The memory location is addressed by state counter 435. The clock pulses are counted by the pulse counter 438 so that the total can be input into memory 434. After the data is verified, receiver unit 500 transmits a carrier signal to increment sensor unit 400 to receive the next digit. The second digit is transmitted as four clock pulses. The first two pulses are an activation signal which change sensor unit 400 to the next state; the last two pulses represent the number two. This procedure is repeated until all data is written in sensor unit 400.

Detailed Description Text (122):
Again, other data can be written to sensor unit 400 in other states. The procedure of activation signals and carrier signals for specific times can be used to reach various states. The following are examples of other data that could be written in these other states: filling sight data, barometric pressure data, date data, last reading data, etc.

Detailed Description Text (123):
The following is a detailed description of the communications explained in reference to sensor unit 400. When the first activation signal is received as in the first part of read signal 620, sensor unit 400 is turned ON. Detector 448 generates two electric pulses which are received by power switch 450. In response to these two pulses power switch 450 holds power source transistor 454 ON for a period of time. Power switch 450 holds power source transistor 454 ON after receiving any subsequent carrier on signals or pulses from detector 448.

Detailed Description Text (124):
Upon activation of sensor unit 400, state counter 435 is cleared by the state clear circuit 436. State counter 435 keeps track of states for read modes and write modes. When the state counter 435 is cleared, the sensor unit 400 is in the read mode, state 1 or the state for reading pressure data. State clear circuit 436 is comprised of a resistor capacitor network employed to provide a pulse upon the activation of sensor unit 400. Alternatively, state clear circuit 436 could be a one shot circuit which provides a pulse when sensor unit 400 is turned ON. State counter 436 has an input which sets the counter at zero when a particular input is placed upon the clear counter input. This method for clearing a counter circuit upon device start-up is known in the art.

Detailed Description Text (129):
A multiplexer 432 selects which signals are transmitted by infrared output circuit 460. Multiplexer 432 has two data inputs; the first data input 432A is connected to analog to digital converter 426, and second data input 432b is connected to memory 434. Multiplexer 432 also has at least 1 control input for selecting the data to output. A control input 432c is connected to state counter 435. Preferably, multiplexer 432 has enough control inputs to select the number of sources. In this exemplary embodiment, an OR gate is connected to all the outputs of state counter 435 so that the digital to analog converter is only chosen when state counter 435 outputs a zero. When the state counter 435 outputs a zero, sensor unit 400 is in the read mode state 1 or the read mode for pressure data. When the output is not zero, the multiplexer 432 selects input 432B.

Detailed Description Text (130):
State counter 453 also is connected to memory 434. Depending upon the state, state counter selects various memory locations in memory 434. Memory 434 preferably has parallel memory outputs connected to shift register for serially transmitting data to the multiplexer 432. Alternatively, memory 432 could be a memory device with a serial output or a serial memory device.

Detailed Description Text (131):
Infrared output circuit 460 produces infrared signals in a similar manner to transmitter circuit 540. A signal is transmitted to input 462a of a NAND gate 462 from multiplexer 432. An oscillator 469 provides a 38 kHz carrier signal to the input 462b of NAND gate 462. If the signal to input 462a is high, an inverted carrier signal is output from NAND gate 462. If the signal to input 462a is LOW, the output of NAND gate 462 is HIGH. When the output of NAND gate 462 is low, a transistor 468 is turned on and current travels through infrared LED 465 and a resistor 467.

Detailed Description Text (133):
The 38 kHz modulated signal is transmitted to receiver circuit 580 in receiver unit 500. Receiver circuit 580 is similar to infrared detector circuit 441 in sensor unit 400. An infrared sensor 582 produces an electrical signal in response to infrared light in proportion to the amount of light received. The amplifier 584 increases the magnitude of the signal produced by infrared sensor 582. The band pass filter 586 prevents signals of inappropriate frequencies from passing to decoder 588. In a preferred embodiment, band pass filter 586 is tuned to 38 kHz so that only signals from sensor unit 400 are allowed to pass. The reason for the

different transmit and receive carrier frequencies is to avoid cross coupling of information between receiver unit 500 and sensor unit 400. If cross coupling exists, sensor unit 500 could remain "ON" by inducing a signal from its own infrared output 460 into its own infrared detector circuit 441. The decoder 588 demodulates the signals from filter 586 and generates electric signals. These signals are input into micro & peripheral circuit 524 for appropriate storage or actions.

Detailed Description Text (134):
Once state counter 435 reaches the write mode through write signals, pulse counter 438 counts pulses sent by receiver unit 500. Pulse counter 438 has outputs connected to memory 434. The data on these outputs is indicative of the number of pulses sent by receiver 500; this data is written to memory 434 after the last pulse is transmitted for the particular state. After the data is written, pulse counter 438 is cleared.

Detailed Description Text (136):
With reference to FIG. 12, write signal 640 is received by sensor unit 400 as sensor write signal 650. Sensor write signal 650 initiates a state change by sending an activation signal followed by a specified period of carrier "ON" signal. In response to this period of carrier signals, state counter 435 is incremented to change states. When the appropriate state is reached by state counter 435, data is transmitted in the form of clock pulses by receiver unit 500.

Detailed Description Text (138):
There are various ways of employing processor circuitry 430 so that it addresses various memory locations, interprets data, stores data, and transmits data. This is a preferred embodiment among various embodiments including a microprocessor based system, or integrated circuit system which do not escape the spirit of the invention as discussed in the claims.

Detailed Description Text (139):
Although this particular preferred embodiment of communication has been described, various other communication techniques, and protocols are available without detracting from the spirit of the invention. For instance activation, deactivation, mode changes, and state changes could be communicated by transmitting different pulses, different frequencies, different pulse widths, different transmitters, or any other distinguishing signals.

Detailed Description Text (142):
Receiver unit 500 also generates time and date data indicative of the time and date of the inspection. This data could be generated by a timer unit (not shown) or inputted by the user through serial port 528 or keyboard 526. The data produced by receiver 500 is stored with data received from sensor unit 400 in memory 522. Memory 522 is large enough to accommodate the relevant data for at least one inspection tour. The data stored in memory 522 can be viewed on display 532 or transmitted through serial port 528 to a central computer.

Detailed Description Text (147):
The remote sensing and receiving system provides an ideal apparatus for checking piping 325 in units as they progress down the assembly line. For example, a production system could be configured so that an air conditioner employed with at least one sensor unit 400 travels along an assembly line and passes by receiver unit 500 situated near the assembly line. Receiver unit 500 is configured to derive power from the assembly line power supply. Receiver unit 500 reads the pressure data transmitted by sensor unit 400. Receiver unit 500 transmits this data to a central computer or other assembly line apparatus so that appropriate action may be taken with regard to the amount of coolant in the air conditioner.

Detailed Description Text (150):

With reference to FIG. 17, the remote sensing and receiving system could also be used in liquid propane tanks. This embodiment is similar to the fire extinguisher embodiment discussed in great detail above. Sensor unit 400 could be affixed in a liquid propane tank 320. Receiver unit 500 would read the pressure data transmitted by sensor unit 400 in a manner similar to the methods discussed in the above other embodiments.

Detailed Description Text (152):
With reference to FIG. 18, receiver unit 2000 includes an infrared receiver 2100, a transmitter circuit 2200, a computer circuit 2300, and a power circuit 2400. These circuits are coupled to each other to perform various receiving operations.

Detailed Description Text (153):
Computer circuit 2300 provides storage and manipulation of data received from infrared receiver 2100. Computer circuit 2300 supplies data to, and controls transmitter circuit 2200. computer circuit 2300 includes a micro and peripheral circuit 2320 and an LCD display 2310. Circuit 2320 receives signals from the infrared receiver 2100 and provides data to LCD display 2310 for generating visual indicia of sensor measurements.

Detailed Description Text (155):
In response to the demodulated signal, computer circuit 2300 applies a control signal to transmitter circuit 2200. The control signal enables and disables a 19 kHz oscillator signal produced by an oscillator 2210. The oscillator signal is applied to an AND gate 2220. AND gate 2200 outputs the oscillator signal when computer circuit 2300 applies a logic "1" to AND gate 2220. When enabled, AND gate 2220 modulates an NPN transistor 2230 at 19 kHz through a resistor 2260. NPN transistor 2230 conducts current through a resistor 2250 and an infrared LED 2240 in response to the signal from AND gate 2220. Infrared LED 2240 emits infrared light in response to the electric signal.

Detailed Description Text (156):
Power circuit 2400 provides electrical power to receiver unit 2000. A 9-volt battery 2420 provides power through a switch 2410 to a 5-volt regulator 2430. 5-volt regulator 2430 provides a 5-volt signal to the infrared receiver 2100, transmitter circuit 2200, and computer circuit 2300.

Detailed Description Text (157):
With reference to FIG. 20, sensor unit 1000 includes an infrared receiver 1100, a transmitter circuit 1200, a pressure measurement circuit 1300, a power circuit 1400, and an activation circuit 1500. The operations of these circuits are similar to the operations of the circuits in receiver unit 2000. These circuits are coupled to each other to perform various operations.

Detailed Description Text (158):
Infrared receiver 1100 is similar to infrared receiver 2100. An infrared detector 1110 produces electric signals in response to infrared signals. A gain amplifier 1120 amplifies the electric signal from infrared detector 1110. A band pass filter 1130 is tuned so that only signals of approximately 19 kHz are allowed to pass from amplifier 1120 to a detector 1140. Detector 1140 demodulates the signal and provides signals such as an A/D data clock signal to activation circuit 1500 and pressure measurement circuit 1300.

Detailed Description Text (159):
Transmitter circuit 1200 is similar to transmitter circuit 2200. Transmitter circuit 1200 is controlled by pressure measurement circuit 1300. An oscillator 1210 provides a 38 kHz signal to one input of a NAND gate 1220. Pressure measurement circuit 1300 provides a signal representing pressure measurement data to a second input of NAND gate 1220. When transmitter circuit 1200 is enabled by pressure measurement circuit 1300, NAND gate 1220 provides the 38 kHz oscillator signal to a

PNP transistor 1230. This signal modulates PNP transistor 1230 at 38 kHz . In response to this modulation, current travels through infrared diode 1240 and a resistor 1250. When current travels through infrared diode 1240, infrared light is emitted.

Detailed Description Text (160):
Power circuit 1400 provides power to the sensor unit 1000. Power circuit 1400 includes a switch 1420 and a battery 1410. Battery 1410 may be a 6-volt lithium battery. Switch 1420 is a one time activated switch which protects battery 1410 from providing power during the manufacture of sensor unit 1000.

Detailed Description Text (161):
Activation circuit 1500 provides power to pressure measurement circuit 1300 when an activation signal, or start-up signal, is provided to a power switch 1510. Power switch 1510 may be a retriggerable monostable circuit. In this particular embodiment, a start-up signal is an infrared 19 kHz modulated signal. The start-up signal can be a pulse or constant "ON" signal of the 19 kHz carrier signal. In response to a start-up signal, power switch 1510 turns a PNP transistor 1530 "ON" and sends a signal to a one shot circuit 1520. One shot circuit 1530 produces an A/D convert signal in response to the signal from power switch 1510. When transistor 1530 is "ON", power is provided to pressure measurement circuit 1300 and transmitter 1200. When transistor 1530 is "OFF", power is only provided to activation circuit 1500 and infrared receiver 1100. Disabling power to circuit 1200 and circuit 1300 increases the life of battery 1410.

Detailed Description Text (162):
When pressure measurement circuit 1300 is provided power by activation circuit 1500, pressure measurement circuit 1300 generates a signal indicative of pressure and provides the signal to transmitter circuit 1200. Pressure measurement circuit 1300 includes a pressure sensor 1320, a pressure transducer 1310, an amplifier 1330, and an analog-to-digital converter 1340.

Detailed Description Text (163):
Pressure sensor 1320 produces an electrical signal indicative of pressure sensed by pressure transducer 1310. This electrical signal is amplified by amplifier 1330. Amplifier 1330 provides temperature compensation and gain amplification. Analog to digital converter 1340 converts the analog pressure signal from amplifier 1330 into a binary signal in response to the A/D convert signal produced by one shot 1520. In response to A/D data clock signal, analog to digital converter 1340 serially outputs the binary signal to transmitter circuit 1200 for eventual reception by receiver unit 2000.

Detailed Description Text (164):
The general operations of receiver unit 2000 and sensor unit 1000 are similar to the general operations of sensor unit 400 and receiver unit 500 discussed previously with reference to FIGS. 10 and 11. With reference to FIGS. 18 and 20, a start-up signal is initiated by computer circuit 2300 and transmitted by transmitter circuit 2100.

Detailed Description Text (165):
The start-up signal is received by infrared receiver 1100. In response, infrared receiver 1100 provides this signal to activation circuit 1500. In response to this signal, activation circuit 1500 provides power to circuits 1200 and 1300. In response to the supply of power and the A/D convert signal, pressure measurement circuit 1300 generates an electric signal indicative of pressure.

Detailed Description Text (166):
In response to clock signals transmitted by receiver unit 2000, transmitter circuit 1200 transmits an infrared signal to receiver unit 2000, where the signal is indicative of the electric signal produced by pressure measurement circuit 1300.

Upon detection of the infrared signal, infrared receiver 2100 generates an electric signal indicative of the infrared signal and transmits the electric signal to computer circuit 2300 to produce a display signal applied to LCD display 2310.

Detailed Description Text (170):
Microprocessor 2322 is coupled to a liquid crystal display (LCD) 2312 by an LCD display controller 2334. Data lines 2350 and 2352 couple microprocessor 2322 to controller 2334, and controller 2334 is coupled to LCD 2312 by data bus 2354. Microprocessor 2322 provides signals to LCD 2312 via controller 2334. LCD 2312 is a LXD 3-digital display mode 30 manufactured by LXD. The LXD mode 30 is chosen for low cost and low power consumption. Other manufacturers of similar devices are available, such as optrex. Controller 2334 drives LCD 2312 in response to signals from microprocessor 2322. Controller 2334 may be a Signetics PCF8577. The Signetics PCF8577 may be chosen since the I2C bus protocol is built into controller 2334. A 680 pF ceramic disk capacitor 2336 and a 1 M ohm resistor 2338 provide a "power on reset" circuit for controller 2334. The details of the interaction and interconnections of microprocessor 2322, LCD 2312, and controller 2334 are explained in the product literature of each device.

Detailed Description Text (171):
Microprocessor 2322 enables transmitter circuit 2200 to emit 19 KHz modulated infrared signals. A 100K ohm resistor 2218, a 0.0018 microfarad ceramic disk capacitor 2214, and a NAND gate 2212 produce a 19 kHz signal. NAND gate 2212 is a 14093 Schmidt NAND gate produced by Motorola or equivalent. (All NAND gates of the second embodiment are of this type.) The charging and discharging of capacitor 2214 and resistor 2218 create the 19 kHz output from NAND gate 2212.

Detailed Description Text (172):
Microprocessor 2322 is coupled to a NAND gate 2224 by data line 2356, where the output of NAND gate 2212 is also connected to gate 2224. NAND gate 2224 allows microprocessor 2322 to selectively apply the 19 kHz signal to a NAND gate 2222. When NAND gate 2224 is enabled by the P3.0 output of microprocessor 2322, the 19 kHz signal is provided to a NAND gate 2222. NAND gate 2222 acts as an invertor. The signal output from NAND gate 2222 is transmitted through a 4.7K ohm resistor 2260 to the base of NPN transistor 2230. NPN transistor 2230 is a 2N4401 transistor produced by Motorola or equivalent.

Detailed Description Text (179):
The 5 volt regulated supply voltage, VCC, and 9 volt supply, +9 volt, are provided through switch 2410 to the circuits in receiver unit 2000. Switch 2410 is suitably a push button switch or an ON-OFF switch. A zener diode 2414 is used to provide a regulated 5-volt voltage. Zener diode 2414 is a 1NS230, a 4.7 volt zener diode or equivalent. A resistor 2412 is a 100 ohm resistor, and switch 2410 is a SPST activation switch. A 47 uF electrolytic capacitor 2416 also filters and regulates the 5-volt voltage.

Detailed Description Text (206):
After sensor unit 1000 has been turned "ON", receiver unit 2000 awaits a predetermined amount of time for shift register 1352 to obtain a binary number indicative of the pressure measured. After this time has elapsed, microprocessor 2322 emits a clock pulse from output P3.0 in response to the software. As described with reference to the start-up pulses, NAND gate 2224 provides a pulse of 19 kHz in response to the clock pulse from microprocessor 2322. This clock pulse is transmitted as a 19 kilohertz modulated infrared pulse from LED 2240. As with the start-up signals, the clock signal is received by infrared detector 1110. In response to this signal, infrared preamplifier 1102 provides an inverted pulse on its pin 9 output. This pulse keeps sensor unit 1000 "ON" by triggering the retriggerable monostable circuit.

Detailed Description Text (207):

This pulse is also provided to NAND gate 1108 which acts as an invertor. NAND gate 1108 produces clock pulses in response to the change of output on pin 9 of infrared preamplifier 1102. This pulse is transmitted across resistor 1362. Resistor 1362 and capacitor 1364 provide a filter for the pulse. This filter eliminates any pulses of insufficient duration and therefore protects against inconsequential receptions by infrared detector 1110. The signal from NAND gate 1108 is provided to the clock input of serial shift register 1352 and is called the Clock In signal. In response to the Clock In signal, shift register 1352 provides the logic level of the most significant bit at output QH. Output QH is provided to NAND gate 1221. As stated previously, infrared LED 1240 provides infrared light modulated at 38 kHz if the NAND gate 1221 is provided with a logic "1" from serial shift register 1352.

Detailed Description Text (216):
In a read sequence, receiver unit 2000 activates sensor unit 1000 with infrared read transmission carrier frequency (step 3110). The analog-to-digital conversion will begin in sensor unit 1000. Next, receiver unit 2000 clocks out the 8 bits of data from serial shift register 1352 (step 3120). Sensor unit 1000 sends a 38 kHz carrier frequency which are detected by receiver unit 2000. Receiver unit 2000 verifies the signal from sensor unit 1000 (step 3130). If the value is verified, receiver unit 2000 stores the value (step 3140). If the signal is not verifiable, receiver unit 2000 clocks the data from sensor unit 1000 (step 3120). After the measurement is stored, the read count value is incremented (step 3150). Receiver unit 2000 ceases sending activation signals after the value is stored (step 3160). Receiver unit 2000 waits for the deactivation time to be reached. In response to the absence of activation signals for 125 milliseconds, sensor unit 1000 is turned "OFF" (step 3170).

Detailed Description Text (225):
Receiver units 2000 provide the pressure data to a large display situated so that the driver can read the display from cab 3020 of truck 3000. The display may be employed as red and green lights so that a red light is illuminated if any sensor 1000 transmits an unsafe pressure value. If all sensor units 1000 transmit safe pressure values, a green light is illuminated. This application is desirable in light of the stricter regulations regarding truck tire pressures on highways.

Detailed Description Text (229):
It will be understood that while the various conductors/connectors may be depicted in the drawings as single lines, they are not shown in a limiting sense and may comprise plural conductors/connectors as understood in the art. Further, the above description is of preferred exemplary embodiments of the present invention; the invention is not limited to the specific forms shown. For example, while sensor unit 400 has been shown, it is understood that various sensing devices could be substituted. In addition, the transducer circuit need not have an independent power source; rather, power may be delivered from the transmitter unit to the transducer unit, as desired. Further still, the invention has been described with reference to block diagrams. These function blocks can be combined into the same device or separated into different discrete devices. For instance, the entire sensor unit 400 could be implemented as one integrated chip. These and other modifications may be made in the design and arrangement of the elements discussed herein without departing from the scope of the invention as expressed in the appended claims.

CLAIMS:

1. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a display unit in remote communication with the sensor unit and being operable for selectively transmitting the command signal to the sensor unit, for receiving from the sensor unit the response signal indicative of the parameter, and for displaying information relating to the parameter.

4. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a transmitting and receiving unit in remote communication with the sensor unit and being operable for selectively transmitting the command signal to the sensor unit, for receiving from the sensor unit the response signal indicative of the parameter, and for enabling the display of information relating to the parameter.

7. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a display unit in remote communication with the sensor unit and being operable for transmitting the command signal to the sensor unit in response to an indication from a user for a sensor reading, for receiving from the sensor unit the response signal indicative of the parameter, and for displaying information relating to the parameter.

10. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a transmitting and receiving unit in remote communication with the sensor unit and being operable for selectively transmitting the command signal to the sensor unit in response to an indication from a user for a sensor reading, for receiving from the sensor unit the response signal indicative of the parameter, and for processing information conveyed in the response signal.

13. The system of claim 10, wherein the transmitting and receiving unit enables information related to the parameter to be displayed.

14. In a system comprising a sensor unit operatively coupled to a vessel and in remote communication with a receiving unit, a method for obtaining information related to a parameter of a vessel, the method comprising: receiving at the receiving unit an indication from a user to activate the sensor unit; remotely activating the sensor unit in response to receiving the indication; obtaining information related to the parameter with the sensor unit; sending a signal indicative of the parameter from the sensor unit to the receiving unit; and receiving the signal at the receiving unit.

17. A method of receiving and displaying information in a display unit, wherein the information is conveyed in a signal transmitted from a sensor unit physically separate from the display unit, the method comprising the steps of: receiving an indication from the user to activate the sensor unit; in response to receiving the indication from the user, remotely activating the sensor unit; remotely receiving the signal from the activated sensor unit; conditioning the signal for display; and displaying information conveyed in the signal.

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DOCUMENT-IDENTIFIER: US 6672151 B1
TITLE: Apparatus and method for remote sensing and receiving

Abstract Text (1):
A sensing and displaying system is provided including a sensor unit having a transducer disposed in intimate contact with a vessel. The transducer senses a characteristic within the vessel like pressure and outputs an electrical signal representative thereof. The sensor unit further includes a response signal generator which transmits a signal representative of the characteristic. A receiver unit receives the transmitted signal and converts it to visual indicia of the characteristic, for example, a number on a liquid crystal display. The system is capable of two-way communication between the sensor unit and the receiver unit. Both the sensor unit and receiver unit store transmitted data in internal memory.

Brief Summary Text (2):
The present invention relates, generally, to a transmitter and receiver combination for measuring a parameter, pressure, force, or weight, within a vessel, and more particularly, to a sensor unit including a transducer and an infrared generator cooperating therewith, for transmitting infrared signals to a remote receiver unit including a measurement display.

Brief Summary Text (10):
The present invention provides a remote sensing and receiving system including a sensor unit and a remote receiver unit. The sensor unit includes a transducer disposed to sense the physical parameter of an apparatus. The transducer generates an electric signal representative of the magnitude of the physical parameter and applies this signal to an LED driver. The LED driver modulates an LED, which transmits an infrared (IR) signal.

Brief Summary Text (12):
The present invention also can be configured to allow for two-way communication between the sensor unit and remote receiver unit. The receiver unit controls the sensor unit by transmitting activation signals for turning the sensor unit on, reading signals for requesting data from the sensor unit, and writing signals for transmitting data to the sensor unit. The sensor and the receiver unit each have a transmitter and a receiver to enable communication through pulses of carrier signals. The data communicated can be stored in memory in the sensor unit or the receiver unit.

Drawing Description Text (3):
FIG. 1 is a schematic representation of a remote display unit and a transmitter unit, including a transducer mounted on a conventional vehicle tire;

Drawing Description Text (11):
FIGS. 12 and 13, are representations of communication signals transmitted and received by the sensor unit and receiver unit;

Detailed Description Text (5):
Pressure sensor unit 16 is advantageously configured to sense tire pressure,

generate an electrical signal indicative of the sensed pressure, and apply the signal to signal converter 34. signal converter 34 converts the pressure signal into an encoded form suitable for use as a modulating signal for LED 38, i.e., LED 38 is modulated in a manner which represents the sensed pressure as a selected characteristic of the encoded signal, e.g., frequency, pulse code, pulse width, etc. Signal converter 34 includes a suitable encoder, such as, for example, a voltage-to-frequency converter, an analog-to-digital converter, a voltage-to-pulse width converter, or the like, and supporting circuitry.

Detailed Description Text (7):
Referring now to FIG. 2B, display unit 12 includes: a battery circuit 41; an appropriate sensor 42, e.g. an IR sensor; a processor 44; and a conventional display 46. The modulated signal transmitted by LED 38 is received at display unit 12 by sensor 42. The voltage from battery 41 is applied to sensor 42, and is modulated in accordance with the response signal received from transducer circuit 14. The modulated signal is applied to a processor 44, wherein information is extracted from the signal and manipulated into a form suitable for application to display 46. Display 46 generates visual indicia, for example a digital readout, representative of tire pressure. A specific embodiment of display unit 12 will hereinafter be described in more detail in conjunction with FIGS. 3 and 4.

Detailed Description Text (8):
As discussed in greater detail below, the functions performed by the various elements comprising the foregoing schematic circuit diagrams may be implemented in a variety of ways. For example, the functions performed by transducer unit 14 may be embodied in a unitary microchip (integrated circuit) for convenient disposition within the valve stem or valve stem cap of a vehicle tire. The functional elements comprising the display unit 12 may similarly be implemented in a microchip or microprocessor, and incorporated into a hand-held remote control display device.

Detailed Description Text (15):
In response to the application of the pulsed command reference signal to the base of transistor Q2, VCC is applied across respective LEDs D2, D3 and D4. Respective LEDs D2-D4 suitably comprise respective IR emitters, Model No. LD271, manufactured by Seimens-Litronix. Thus, respective LEDs D2.varies.D4, under the control of processor U3, generate emissions modulated with a predetermined frequency (tone). As described in greater detail below, the frequency modulated infrared signal transmitted by command generator 56 comprises a "wake-up" command signal C5 used to activate transducer unit 14. Also as described in greater detail below, transducer unit 14 responsively transmits an infrared signal, indicative of tire pressure, back to display unit 12.

Detailed Description Text (22):
In a preferred embodiment of the present invention, transducer unit 14 is configured for disposition within a modified valve stem cap for use in conjunction with conventional vehicle tire valve stems (see FIG. 9). In this manner, a low cost pressure sensor circuit may be powered by a battery which, upon depletion of power, may be discarded. Nonetheless, it is desirable to construct the transducer circuit such that a minimum amount of power is consumed. Transducer unit 14 therefore preferably operates in alternative "dormant" and "active" states. The active state is triggered by reception of command signal CS from display unit 12.

Detailed Description Text (29):
Transducer 60 suitably comprises an electromechanical transducer capable of generating a low level voltage output, for example between 0 and 10 volts, in response to the application of pressures in the range typically exhibited by vehicle tires, i.e., up to 150 psi. Piezoelectric materials are known to be excellent transducers. Although it is desirable to miniaturize the pressure sensing circuit in the preferred embodiment, a pressure sensor Model No. 24 OPC manufactured by Microswitch has yielded satisfactory results in the laboratory.

Those skilled in the art will appreciate that transducer 60 may comprise a suitable microsensor.

Detailed Description Text (44):
If processor U3 determines that switch S is depressed, the output at pin 39 is enabled, thereby applying the command reference signal to command generator circuit 56 and transmitting command signal CS to transducer circuit 52 (step 110).

Detailed Description Text (67):
Pressure transducer 60 (not shown in FIG. 9) is suitably housed within housing 172. signal conversion circuitry, such as that described in connection with signal convertor 34 (FIG. 2), is also housed within housing 172. Similarly, the transmitter and transmitter driver components, analogous to LED 38 and LED driver 36 of FIG. 2, may be housed within housing 172. Alternatively, IR unit 168 may perform the dual function of receiving a command signal and transmitting a response signal, in which case sensor 168 may also comprise an appropriate LED (not shown). In yet a further alternate embodiment, the response generator (LED and driver) may be disposed proximate an opening which extends through the side of cap 124 proximate housing. 172.

Detailed Description Text (71):
Sensor unit 400 is affixed to fire extinguisher device 305 preferably near the nozzle 307. A transducer 422 is disposed within the pressurized tank of fire extinguisher 305. Sensor unit 400 is attached in or on fire extinguisher device 305 so that sensor unit 400 can transmit signals via an infrared output 460. Those skilled in the art will appreciate that sensor unit 400 may be mounted in various places so that transducer 422 is exposed to the pressure in the tank of fire extinguisher 305 and infrared output 460 is exposed to the exterior of extinguisher 305.

Detailed Description Text (73):
Sensor unit 400 and a receiver unit 500 are employed in the inspection and maintenance of fire extinguisher devices. In order for proper inspection, sensor unit 400 must be capable of transmitting data to receiver unit 500 indicative of the identification of the fire extinguisher. By way of example, identification data may include an identification number, a filling sight number, the date and time of inspection, and status of the fire extinguisher. Some of this data can be input into a memory 434 at the time fire extinguisher 305 is filled or at the time sensor unit 400 is provided at fire extinguisher 305. This data can also be programmed into memory 434 by receiver unit 500. If memory 434 is powered memory, switch 453 must be closed before loading any data into memory.

Detailed Description Text (77):
In the normal course of building maintenance, an inspector holding receiver unit 500 periodically walks up to fire extinguisher device 305 employed with sensor unit 400. The inspector presses the appropriate keys on a keyboard 526 in order to activate sensor unit 400. In response to the appropriate keys and or switches, receiver unit 500 transmits an activation signal to sensor unit 400. An activation is a signal like a start-up signal which turns on a particular device. In response to this activation signal, sensor unit 400 is turned "ON" and transmits signals indicative of characteristics of fire extinguisher device 305 and sensor unit 400.

Detailed Description Text (79):
Referring now to FIG. 10, sensor unit 400 includes an activation circuit 440, a pressure measurement circuitry 420, a processor circuitry 430, infrared output 460 and battery 410. Activation circuit 440 includes an infrared detector circuit 441, a power switch circuit 450 and a power source transistor 454. Infrared detector circuit 441 includes an infrared sensor 442, a gain amplifier 444, a band pass filter 446, and a detector circuit 448. As is well known in the art, most circuit elements on sensor unit 400 could be reduced and combined with other elements onto

a single microchip. This reduction saves manufacturing time, power requirements, and size.

Detailed Description Text (80):
The interaction the circuits in FIG. 10 are explained generally as follows. Detector circuit 441 detects infrared signals and generates demodulated electric signals. These signals are provided to processor circuitry 430, pressure measurement circuitry 420, and activation circuit 440.

Detailed Description Text (84):
The circuitry in sensor unit 400 generally is in a dormant state until turned "ON" by activation circuit 440. Sensor unit 400 saves energy from battery 410 by operating in the "STANDBY" mode unless communicating with receiver unit 500. In the "STANDBY" mode, all circuitry in sensor 400 is powered down except for infrared detector circuit 441, activation circuit 440, and memory 434. Activation circuit 440 turns remote sensor unit 400 "ON" when activation circuit 440 receives the proper signal from receiver unit 500. In the preferred embodiment the proper signal is 19 kHz carrier signal although sensor unit 400 could be configured for various frequencies. Sensor unit 400 is in a "STANDBY" mode at all other times.

Detailed Description Text (85):
When an activation signal from receiver unit 500 is transmitted to remote sensor unit 400, activation circuit 440 provides a path to power for other circuit elements. Power source transistor 454 is turned on to provide the path to battery 410. The circuit elements that receive power through transistor 454 are processor circuitry 430, pressure measurement circuit 420, and infrared output 460.

Detailed Description Text (87):
The encoded signal indicative of pressure produced by processor circuitry 430 is applied to infrared output circuit 460. An infrared LED 465 is modulated in a manner which represents the sensed pressure as a selected characteristic of the encoded signal, e.g., frequency, pulse code, pulse width, etc. In a preferred embodiment, infrared output circuit 460 drives infrared LED 465, which emits a modulated pulse response signal, suitably in the infrared frequency range, indicative of pressure. The LED emissions are preferably directional so that the inspector can determine which sensor unit 400 is being read by the relative position of receiver unit 500 to sensor unit 400.

Detailed Description Text (88):
Referring now to FIG. 11, receiver unit 500 suitably comprises: a power circuit 510, a computer circuit 520, and a transmitter circuit 540. Power circuit 510 includes a battery 512, a switch 514, and a voltage regulator 516. Switch 514 is a standard user activated switch for turning "ON" the receiver unit 500. Receiver unit also includes a receiver circuit 580.

Detailed Description Text (90):
Computer circuit 520 also is responsible for creating control signals such as read, write, and activations signals. These signals are generated by computer circuit 520 in response to commands form the user or software. These signals are provided to transmitter 540. Transmitter 540 modulates these signals and produces a modulated infrared signal for sensor unit 400.

Detailed Description Text (91):
Receiver unit 500 is advantageously configured to transmit control signals like activation signals, read signals, and write signals. Activation signals cause activation circuit 440 to turn "ON" components in sensor unit 400; read signals cause processor circuitry 430 to initiate generation of signals indicative pressure data or other data by sensor unit 400; write signals cause data transmitted by receiver unit 500 to be stored in memory 434 of sensor unit 400. Computer circuit 520 creates these signals which are transmitted to sensor unit 400. These signals

are initiated by a program stored in memory 522 or from user manipulation of keyboard 526 or other switches.

Detailed Description Text (92):
Computer circuit 520 applies these control or processor signals to transmitter circuit 540. Transmitter circuit 540 modulates an infrared LED 548 in accordance with processor signals or signals initiated by computer circuit 520. Receiver unit 500 communicates processor signals to sensor unit 400 by modulating LED 548 in a particular frequency, pulse code, pulse width, etc. Preferably, infrared LED 548 operates in the infrared frequency range.

Detailed Description Text (98):
A description of the preferred internal operation of the remote sensing and receiving system is described as follows with reference to FIGS. 10, 11, 12 and 13. With switch 514 closed, the operator can initiate an activation signal 610 through keyboard 526 or a program stored in memory 522 or micro & peripheral circuit 524. Activation signal 610 is transmitted as pulses of particular frequency or tone as in signal 612; in a preferred embodiment pulses of a 19 kHz signal provides an activation signal 610. Micro & peripheral circuit 524 creates an activation signal when micro & peripheral circuit 524 enables transmitter circuit 540. Processor circuitry changes the state of an input 541 of the AND gate 544 to a logic high. An input 543 of AND gate 544 is a 19 kHz carrier signal created by an oscillator 542. When input 541 is high, the output of AND gate 544 is the same signal received by input 543; in this embodiment, a 19 kHz carrier signal is transmitted as long as input 541 is high. This signal travels across a resistor 545 and turns a transistor 546 on and off at a frequency of 19 kHz. As transistor 546 is modulated at 19 kHz, a 19 kHz signal travels through infrared LED 548 and a resistor 547. Infrared LED 548 produces an infrared signal modulated at 19 kHz in response to the electrical signal. In other words, a 19 kHz carrier signal of infrared light is produced by infrared LED 548 and transmitted to sensor unit 400.

Detailed Description Text (99):
With reference to FIG. 13, a signal 612, a 19 kHz carrier signal, is demodulated as a signal 614, an ON signal. An activation signal is shown as activation signal 610 or as part of hand-held read signal 620.

Detailed Description Text (100):
When any infrared light is transmitted to sensor unit 400, infrared sensor 442 produces an electric signal proportional to the amount of infrared light received. The electric signal is amplified by gain amplifier 444 and input into band pass filter 446. Band pass filter 446 filters signal eliminating any signals not of the proper frequency. Preferably, band pass filter 446 is tuned so that only 19 kHz signals are transmitted to detector 448. Detector 448 receives the filtered signal and demodulates the 19 kHz carrier signal into clock pulses representing the presence of the carrier signal as represented by signal 612. In other words, detector 448 preferably generates a pulse signal similar to the pulse signal created by micro & peripheral circuit 524 and transmitted to input 541. Detector 448 transmits this pulse signal to power switch circuit 450, pressure measurement circuit 420, and processor circuitry 430. Communications between sensor unit 400 and receiver unit 500 are explained as follows from the perspective of the receiver unit 500.

Detailed Description Text (101):
Power switch circuit 450 turns power source transistor 454 to an "ON" state in response to an activation signal. Power switch circuit 450 keeps power source transistor 454 "ON" for a specific amount of time after a signal. Power source transistor 454 provides a path to power other circuit elements in sensor unit 400. The activation signal must be at least 2 pulses in order to keep the sensor unit 400 in an "ON" mode. The activation signal is chosen as two pulses rather. than one in order to ensure the reliability of signal reception. In the preferred

embodiment, logic circuits and counters are used as part of power switch circuit 450 to turn sensor unit 400 "ON" after receiving the two pulses of activation signal 610. The device can be configured to have various activation signals. For example, a less conservative approach could simply use one pulse to activate sensor unit 400. An activation signal is a necessary part of both read and write signals as is explained below.

Detailed Description Text (102):
Computer circuit 520 creates read signals so that sensor unit 400 transmits data to receiver unit 500. With reference to FIG. 13, read signal 620 is produced by receiver unit 500 upon initiation by operator or program stored in memory 522. The first part of read signal 620 is an activation signal. The rest of read signal 620 are clock pulses which initiate the transmission of data by sensor unit 400.

Detailed Description Text (103):
Read signal 620 is created in the transmitter circuit 540 similarly to activation signal 610. Micro & peripheral circuit 524 sends pulse signals to the input 541 of AND gate 544. In response to this signal, LED 548 is modulated to produce pulses of 19 kHz carrier signals.

Detailed Description Text (104):
In response to this first activation signal, sensor unit 400 is turned "ON". When sensor unit 400 is turned ON from the dormant state or "STANDBY" mode, the sensor unit begins in read mode, state 1. After the activation signal, receiver unit 500 sends clock pulses of 19 kHz carrier signal; these pulses are part of read signal 620.

Detailed Description Text (105):
In the read mode, state 1, sensor unit 400 determines the pressure and transmits pressure data back to receiver unit 500 synchronously with the clock pulses of read signal 620. The pressure data is transmitted in the form of a sensor read signal 624. Once micro & peripheral circuit 524 receives a pulse representing data in sensor read signal 624, receiver unit 500 transmits another pulse. In response to this pulse, sensor unit 400 transmits another pulse representing data. Sensor unit 400 and receiver unit 500 repeat these operations until the requested data is transmitted by sensor unit 400.

Detailed Description Text (108):
When additional information is desired from the sensor unit 400, receiver unit 500 transmits read signals so that sensor unit 400 operates in a different state. Receiver unit 500 changes the state of sensor unit 400 by holding the carrier signals "ON" for a specific length of time without pulses. If the carrier signal is off for a specified length of time, sensor unit 400 will be deactivated; upon start-up, sensor unit 400 begins in the read mode, state 1 again.

Detailed Description Text (110):
After the carrier "ON" signal has been sent for an appropriate length of time, receiver unit 500 transmits an activation signal of at least two pulses so that sensor unit 400 changes states. Sensor unit 400 changes states in response to this activation signal and the pulse signal from charge circuit 431. In the new state, sensor unit 400 transmits new information corresponding to the different state in response to clock pulses from the receiver unit 500.

Detailed Description Text (111):
With reference to FIG. 13, a read signal 630 activates sensor unit 400 "ON" and transmits the carrier signal until state 2 is reached. When state 2 is reached, receiver unit 500 transmits another activation signal followed by the carrier signal to reach state X. When state 2 is surpassed, receiver unit 500 transmits another activation signal followed by clock pulses so that sensor unit 400 transmits data in state X.

Detailed Description Text (112):
In response to the clock pulses, sensor unit 400 synchronously transmits pulses representing information as shown in read signal 630 and the a sensor read signal 632. These clock pulses allow the receiver unit 500 to keep track of the information received. With this method, information is not received out of sequence because each bit of data is transmitted upon initiation of a clock pulse from receiver unit 500. Receiver unit 500 does not send another clock pulse until the requested bit is received. After all the bits making up the requested data are received, receiver unit 500 does not send any more clock pulses.

Detailed Description Text (113):
As an example, when the sensor unit 400 is in the read mode, state X, identification data is transmitted to receiver unit 500. Sensor unit 400 stores the identification data in memory 434. The data is transmitted serially from memory 434 to multiplexer 432. In a particular embodiment, memory 434 includes a shift register for outputting data. State counter 435 addresses the memory location associated with a given state so that memory 435 outputs the data to the shift register. The clock pulses in read signal 630 initiate a serial output of the data one bit at a time by the shift register.

Detailed Description Text (114):
Various states could be reached by sensor unit 400 through the method of activation signals and carrier signals described above. In these various states, various information could be sought and transmitted according to the users needs.

Detailed Description Text (115):
State X is not the limit of states; other states can be reached by the same technique. For instance, activation signals and carrier signals can be transmitted at appropriate times in order to reach read mode, state Y. In state Y, sensor unit 400 synchronously transmits different information in response to pulses transmitted by receiver unit 500. This different information could be stored in a memory location in memory 434 which is addressable by state counter 435. For example, this different information could be the date of the last measurement of pressure. This procedure can be continued in this fashion until all desired information is obtained.

Detailed Description Text (116):
With reference to FIG. 13, read signal 630 shows that different states can be reached without having to transmit data at every previous state. This feature saves energy as LED 465 is not driven unnecessarily. For instance, read signal 630 reaches state X without having sensor unit 400 transmit data in states 1 and 2. Read signal 630 skipped the data in states 1 and 2 by not providing any clock pulses in between activation signals, instead a constant carrier signal was provided. In contrast, read signal 620 provided for the reception of the data of state 1 by transmitting clock pulses after the activation signal.

Detailed Description Text (117):
The write mode is slightly more complicated than the read mode. Unlike the read mode, receiver unit 500 must send specific data to sensor unit 400 in the write sequence. The data is represented by a series of pulses. This data can be location data, identification data, barometric pressure, the date, or any other data for use or storage by sensor unit 400. The series of pulses are generated by processing circuitry 524 and sent through transmitter circuit 540.

Detailed Description Text (118):
With reference to FIG.12, the write mode is reached in sensor unit 400 with activation signals and providing change state signals with carrier signals for a specified amount of time. Preferably, the write mode is after the last state in the read mode. In other words, receiver unit 500 transmits a series of activation

signals followed by carrier signals for a specified length of time until all read states have been surpassed. Once the write mode and proper state is reached, receiver unit 500 sends data corresponding to the state.

Detailed Description Text (119):
Just as the correct state had to be reached in the read mode, the correct state has to be reached for the write mode. For instance, if the operator is transmitting identification data to sensor unit 400, sensor unit 400 should be in the write mode, state X where state X is the state for receiving the first number of the identification.

Detailed Description Text (120):
For example, in order to store identification number 00225, there are five identification states, one for each digit. After the write mode is reached, sensor unit 400 is put in state X by transmitting the write signal 640. Write signal 640 is a combination of an activation signal and carrier signals. After the appropriate mode is reached, the first digit is input by transmitting an activation signal (two clock pulses) and the digit (5 clock pulses). Again, two clock pulses for an activation signal are not required; the circuit can be designed so that one would be sufficient. However, two clock pulses are implemented in this design because two pulses are more reliable. In other words once correct state is reached, receiver unit 500 transmits seven clock pulses. Upon receiving the activation signals, sensor unit 400 synchronously transmits the data back to receiver unit 500 as in the sensor write signal 650. Receiver unit 500 verifies that the data transfer was correct. If the data received was not correct, receiver unit 500 does not advance sensor unit 400 into the next state, and transfers the data again.

Detailed Description Text (121):
In response to the data represented by clock pulses, sensor unit 400 stores the digit five in memory 434 in a space reserved for the first identification number. The memory location is addressed by state counter 435. The clock pulses are counted by the pulse counter 438 so that the total can be input into memory 434. After the data is verified, receiver unit 500 transmits a carrier signal to increment sensor unit 400 to receive the next digit. The second digit is transmitted as four clock pulses. The first two pulses are an activation signal which change sensor unit 400 to the next state; the last two pulses represent the number two. This procedure is repeated until all data is written in sensor unit 400.

Detailed Description Text (122):
Again, other data can be written to sensor unit 400 in other states. The procedure of activation signals and carrier signals for specific times can be used to reach various states. The following are examples of other data that could be written in these other states: filling sight data, barometric pressure data, date data, last reading data, etc.

Detailed Description Text (123):
The following is a detailed description of the communications explained in reference to sensor unit 400. When the first activation signal is received as in the first part of read signal 620, sensor unit 400 is turned ON. Detector 448 generates two electric pulses which are received by power switch 450. In response to these two pulses power switch 450 holds power source transistor 454 ON for a period of time. Power switch 450 holds power source transistor 454 ON after receiving any subsequent carrier on signals or pulses from detector 448.

Detailed Description Text (124):
Upon activation of sensor unit 400, state counter 435 is cleared by the state clear circuit 436. State counter 435 keeps track of states for read modes and write modes. When the state counter 435 is cleared, the sensor unit 400 is in the read mode, state 1 or the state for reading pressure data. State clear circuit 436 is comprised of a resistor capacitor network employed to provide a pulse upon the

activation of sensor unit 400. Alternatively, state clear circuit 436 could be a one shot circuit which provides a pulse when sensor unit 400 is turned ON. State counter 436 has an input which sets the counter at zero when a particular input is placed upon the clear counter input. This method for clearing a counter circuit upon device start-up is known in the art.

Detailed Description Text (129):
A multiplexer 432 selects which signals are transmitted by infrared output circuit 460. Multiplexer 432 has two data inputs; the first data input 432A is connected to analog to digital converter 426, and second data input 432b is connected to memory 434. Multiplexer 432 also has at least 1 control input for selecting the data to output. A control input 432c is connected to state counter 435. Preferably, multiplexer 432 has enough control inputs to select the number of sources. In this exemplary embodiment, an OR gate is connected to all the outputs of state counter 435 so that the digital to analog converter is only chosen when state counter 435 outputs a zero. When the state counter 435 outputs a zero, sensor unit 400 is in the read mode state 1 or the read mode for pressure data. When the output is not zero, the multiplexer 432 selects input 432B.

Detailed Description Text (130):
State counter 453 also is connected to memory 434. Depending upon the state, state counter selects various memory locations in memory 434. Memory 434 preferably has parallel memory outputs connected to shift register for serially transmitting data to the multiplexer 432. Alternatively, memory 432 could be a memory device with a serial output or a serial memory device.

Detailed Description Text (131):
Infrared output circuit 460 produces infrared signals in a similar manner to transmitter circuit 540. A signal is transmitted to input 462a of a NAND gate 462 from multiplexer 432. An oscillator 469 provides a 38 kHz carrier signal to the input 462b of NAND gate 462. If the signal to input 462a is high, an inverted carrier signal is output from NAND gate 462. If the signal to input 462a is LOW, the output of NAND gate 462 is HIGH. When the output of NAND gate 462 is low, a transistor 468 is turned on and current travels through infrared LED 465 and a resistor 467.

Detailed Description Text (133):
The 38 kHz modulated signal is transmitted to receiver circuit 580 in receiver unit 500. Receiver circuit 580 is similar to infrared detector circuit 441 in sensor unit 400. An infrared sensor 582 produces an electrical signal in response to infrared light in proportion to the amount of light received. The amplifier 584 increases the magnitude of the signal produced by infrared sensor 582. The band pass filter 586 prevents signals of inappropriate frequencies from passing to decoder 588. In a preferred embodiment, band pass filter 586 is tuned to 38 kHz so that only signals from sensor unit 400 are allowed to pass. The reason for the different transmit and receive carrier frequencies is to avoid cross coupling of information between receiver unit 500 and sensor unit 400. If cross coupling exists, sensor unit 500 could remain "ON" by inducing a signal from its own infrared output 460 into its own infrared detector circuit 441. The decoder 588 demodulates the signals from filter 586 and generates electric signals. These signals are input into micro & peripheral circuit 524 for appropriate storage or actions.

Detailed Description Text (134):
Once state counter 435 reaches the write mode through write signals, pulse counter 438 counts pulses sent by receiver unit 500. Pulse counter 438 has outputs connected to memory 434. The data on these outputs is indicative of the number of pulses sent by receiver 500; this data is written to memory 434 after the last pulse is transmitted for the particular state. After the data is written, pulse counter 438 is cleared.

Detailed Description Text (136):
With reference to FIG. 12, write signal 640 is received by sensor unit 400 as sensor write signal 650. Sensor write signal 650 initiates a state change by sending an activation signal followed by a specified period of carrier "ON" signal. In response to this period of carrier signals, state counter 435 is incremented to change states. When the appropriate state is reached by state counter 435, data is transmitted in the form of clock pulses by receiver unit 500.

Detailed Description Text (138):
There are various ways of employing processor circuitry 430 so that it addresses various memory locations, interprets data, stores data, and transmits data. This is a preferred embodiment among various embodiments including a microprocessor based system, or integrated circuit system which do not escape the spirit of the invention as discussed in the claims.

Detailed Description Text (139):
Although this particular preferred embodiment of communication has been described, various other communication techniques, and protocols are available without detracting from the spirit of the invention. For instance activation, deactivation, mode changes, and state changes could be communicated by transmitting different pulses, different frequencies, different pulse widths, different transmitters, or any other distinguishing signals.

Detailed Description Text (142):
Receiver unit 500 also generates time and date data indicative of the time and date of the inspection. This data could be generated by a timer unit (not shown) or inputted by the user through serial port 528 or keyboard 526. The data produced by receiver 500 is stored with data received from sensor unit 400 in memory 522. Memory 522 is large enough to accommodate the relevant data for at least one inspection tour. The data stored in memory 522 can be viewed on display 532 or transmitted through serial port 528 to a central computer.

Detailed Description Text (147):
The remote sensing and receiving system provides an ideal apparatus for checking piping 325 in units as they progress down the assembly line. For example, a production system could be configured so that an air conditioner employed with at least one sensor unit 400 travels along an assembly line and passes by receiver unit 500 situated near the assembly line. Receiver unit 500 is configured to derive power from the assembly line power supply. Receiver unit 500 reads the pressure data transmitted by sensor unit 400. Receiver unit 500 transmits this data to a central computer or other assembly line apparatus so that appropriate action may be taken with regard to the amount of coolant in the air conditioner.

Detailed Description Text (150):
With reference to FIG. 17, the remote sensing and receiving system could also be used in liquid propane tanks. This embodiment is similar to the fire extinguisher embodiment discussed in great detail above. Sensor unit 400 could be affixed in a liquid propane tank 320. Receiver unit 500 would read the pressure data transmitted by sensor unit 400 in a manner similar to the methods discussed in the above other embodiments.

Detailed Description Text (152):
With reference to FIG. 18, receiver unit 2000 includes an infrared receiver 2100, a transmitter circuit 2200, a computer circuit 2300, and a power circuit 2400. These circuits are coupled to each other to perform various receiving operations.

Detailed Description Text (153):
Computer circuit 2300 provides storage and manipulation of data received from infrared receiver 2100. Computer circuit 2300 supplies data to, and controls

transmitter circuit 2200. computer circuit 2300 includes a micro and peripheral circuit 2320 and an LCD display 2310. Circuit 2320 receives signals from the infrared receiver 2100 and provides data to LCD display 2310 for generating visual indicia of sensor measurements.

Detailed Description Text (155):
In response to the demodulated signal, computer circuit 2300 applies a control signal to transmitter circuit 2200. The control signal enables and disables a 19 kHz oscillator signal produced by an oscillator 2210. The oscillator signal is applied to an AND gate 2220. AND gate 2200 outputs the oscillator signal when computer circuit 2300 applies a logic "1" to AND gate 2220. When enabled, AND gate 2220 modulates an NPN transistor 2230 at 19 kHz through a resistor 2260. NPN transistor 2230 conducts current through a resistor 2250 and an infrared LED 2240 in response to the signal from AND gate 2220. Infrared LED 2240 emits infrared light in response to the electric signal.

Detailed Description Text (156):
Power circuit 2400 provides electrical power to receiver unit 2000. A 9-volt battery 2420 provides power through a switch 2410 to a 5-volt regulator 2430. 5-volt regulator 2430 provides a 5-volt signal to the infrared receiver 2100, transmitter circuit 2200, and computer circuit 2300.

Detailed Description Text (157):
With reference to FIG. 20, sensor unit 1000 includes an infrared receiver 1100, a transmitter circuit 1200, a pressure measurement circuit 1300, a power circuit 1400, and an activation circuit 1500. The operations of these circuits are similar to the operations of the circuits in receiver unit 2000. These circuits are coupled to each other to perform various operations.

Detailed Description Text (158):
Infrared receiver 1100 is similar to infrared receiver 2100. An infrared detector 1110 produces electric signals in response to infrared signals. A gain amplifier 1120 amplifies the electric signal from infrared detector 1110. A band pass filter 1130 is tuned so that only signals of approximately 19 kHz are allowed to pass from amplifier 1120 to a detector 1140. Detector 1140 demodulates the signal and provides signals such as an A/D data clock signal to activation circuit 1500 and pressure measurement circuit 1300.

Detailed Description Text (159):
Transmitter circuit 1200 is similar to transmitter circuit 2200. Transmitter circuit 1200 is controlled by pressure measurement circuit 1300. An oscillator 1210 provides a 38 kHz signal to one input of a NAND gate 1220. Pressure measurement circuit 1300 provides a signal representing pressure measurement data to a second input of NAND gate 1220. When transmitter circuit 1200 is enabled by pressure measurement circuit 1300, NAND gate 1220 provides the 38 kHz oscillator signal to a PNP transistor 1230. This signal modulates PNP transistor 1230 at 38 kHz . In response to this modulation, current travels through infrared diode 1240 and a resistor 1250. When current travels through infrared diode 1240, infrared light is emitted.

Detailed Description Text (160):
Power circuit 1400 provides power to the sensor unit 1000. Power circuit 1400 includes a switch 1420 and a battery 1410. Battery 1410 may be a 6-volt lithium battery. Switch 1420 is a one time activated switch which protects battery 1410 from providing power during the manufacture of sensor unit 1000.

Detailed Description Text (161):
Activation circuit 1500 provides power to pressure measurement circuit 1300 when an activation signal, or start-up signal, is provided to a power switch 1510. Power switch 1510 may be a retriggerable monostable circuit. In this particular

embodiment, a start-up signal is an infrared 19 kHz modulated signal. The start-up signal can be a pulse or constant "ON" signal of the 19 kHz carrier signal. In response to a start-up signal, power switch 1510 turns a PNP transistor 1530 "ON" and sends a signal to a one shot circuit 1520. One shot circuit 1530 produces an A/D convert signal in response to the signal from power switch 1510. When transistor 1530 is "ON", power is provided to pressure measurement circuit 1300 and transmitter 1200. When transistor 1530 is "OFF", power is only provided to activation circuit 1500 and infrared receiver 1100. Disabling power to circuit 1200 and circuit 1300 increases the life of battery 1410.

Detailed Description Text (162):
When pressure measurement circuit 1300 is provided power by activation circuit 1500, pressure measurement circuit 1300 generates a signal indicative of pressure and provides the signal to transmitter circuit 1200. Pressure measurement circuit 1300 includes a pressure sensor 1320, a pressure transducer 1310, an amplifier 1330, and an analog-to-digital converter 1340.

Detailed Description Text (163):
Pressure sensor 1320 produces an electrical signal indicative of pressure sensed by pressure transducer 1310. This electrical signal is amplified by amplifier 1330. Amplifier 1330 provides temperature compensation and gain amplification. Analog to digital converter 1340 converts the analog pressure signal from amplifier 1330 into a binary signal in response to the A/D convert signal produced by one shot 1520. In response to A/D data clock signal, analog to digital converter 1340 serially outputs the binary signal to transmitter circuit 1200 for eventual reception by receiver unit 2000.

Detailed Description Text (164):
The general operations of receiver unit 2000 and sensor unit 1000 are similar to the general operations of sensor unit 400 and receiver unit 500 discussed previously with reference to FIGS. 10 and 11. With reference to FIGS. 18 and 20, a start-up signal is initiated by computer circuit 2300 and transmitted by transmitter circuit 2100.

Detailed Description Text (165):
The start-up signal is received by infrared receiver 1100. In response, infrared receiver 1100 provides this signal to activation circuit 1500. In response to this signal, activation circuit 1500 provides power to circuits 1200 and 1300. In response to the supply of power and the A/D convert signal, pressure measurement circuit 1300 generates an electric signal indicative of pressure.

Detailed Description Text (166):
In response to clock signals transmitted by receiver unit 2000, transmitter circuit 1200 transmits an infrared signal to receiver unit 2000, where the signal is indicative of the electric signal produced by pressure measurement circuit 1300. Upon detection of the infrared signal, infrared receiver 2100 generates an electric signal indicative of the infrared signal and transmits the electric signal to computer circuit 2300 to produce a display signal applied to LCD display 2310.

Detailed Description Text (170):
Microprocessor 2322 is coupled to a liquid crystal display (LCD) 2312 by an LCD display controller 2334. Data lines 2350 and 2352 couple microprocessor 2322 to controller 2334, and controller 2334 is coupled to LCD 2312 by data bus 2354. Microprocessor 2322 provides signals to LCD 2312 via controller 2334. LCD 2312 is a LXD 3-digital display mode 30 manufactured by LXD. The LXD mode 30 is chosen for low cost and low power consumption. Other manufacturers of similar devices are available, such as optrex. Controller 2334 drives LCD 2312 in response to signals from microprocessor 2322. Controller 2334 may be a Signetics PCF8577. The Signetics PCF8577 may be chosen since the I2C bus protocol is built into controller 2334. A 680 pF ceramic disk capacitor 2336 and a 1 M ohm resistor 2338 provide a "power on

reset" circuit for controller 2334. The details of the interaction and interconnections of microprocessor 2322, LCD 2312, and controller 2334 are explained in the product literature of each device.

Detailed Description Text (171):
Microprocessor 2322 enables transmitter circuit 2200 to emit 19 KHz modulated infrared signals. A 100K ohm resistor 2218, a 0.0018 microfarad ceramic disk capacitor 2214, and a NAND gate 2212 produce a 19 kHz signal. NAND gate 2212 is a 14093 Schmidt NAND gate produced by Motorola or equivalent. (All NAND gates of the second embodiment are of this type.) The charging and discharging of capacitor 2214 and resistor 2218 create the 19 kHz output from NAND gate 2212.

Detailed Description Text (172):
Microprocessor 2322 is coupled to a NAND gate 2224 by data line 2356, where the output of NAND gate 2212 is also connected to gate 2224. NAND gate 2224 allows microprocessor 2322 to selectively apply the 19 kHz signal to a NAND gate 2222. When NAND gate 2224 is enabled by the P3.0 output of microprocessor 2322, the 19 kHz signal is provided to a NAND gate 2222. NAND gate 2222 acts as an invertor. The signal output from NAND gate 2222 is transmitted through a 4.7K ohm resistor 2260 to the base of NPN transistor 2230. NPN transistor 2230 is a 2N4401 transistor produced by Motorola or equivalent.

Detailed Description Text (179):
The 5 volt regulated supply voltage, VCC, and 9 volt supply, +9 volt, are provided through switch 2410 to the circuits in receiver unit 2000. Switch 2410 is suitably a push button switch or an ON-OFF switch. A zener diode 2414 is used to provide a regulated 5-volt voltage. Zener diode 2414 is a 1NS230, a 4.7 volt zener diode or equivalent. A resistor 2412 is a 100 ohm resistor, and switch 2410 is a SPST activation switch. A 47 uF electrolytic capacitor 2416 also filters and regulates the 5-volt voltage.

Detailed Description Text (206):
After sensor unit 1000 has been turned "ON", receiver unit 2000 awaits a predetermined amount of time for shift register 1352 to obtain a binary number indicative of the pressure measured. After this time has elapsed, microprocessor 2322 emits a clock pulse from output P3.0 in response to the software. As described with reference to the start-up pulses, NAND gate 2224 provides a pulse of 19 kHz in response to the clock pulse from microprocessor 2322. This clock pulse is transmitted as a 19 kilohertz modulated infrared pulse from LED 2240. As with the start-up signals, the clock signal is received by infrared detector 1110. In response to this signal, infrared preamplifier 1102 provides an inverted pulse on its pin 9 output. This pulse keeps sensor unit 1000 "ON" by triggering the retriggerable monostable circuit.

Detailed Description Text (207):
This pulse is also provided to NAND gate 1108 which acts as an invertor. NAND gate 1108 produces clock pulses in response to the change of output on pin 9 of infrared preamplifier 1102. This pulse is transmitted across resistor 1362. Resistor 1362 and capacitor 1364 provide a filter for the pulse. This filter eliminates any pulses of insufficient duration and therefore protects against inconsequential receptions by infrared detector 1110. The signal from NAND gate 1108 is provided to the clock input of serial shift register 1352 and is called the Clock In signal. In response to the Clock In signal, shift register 1352 provides the logic level of the most significant bit at output QH. Output QH is provided to NAND gate 1221. As stated previously, infrared LED 1240 provides infrared light modulated at 38 kHz if the NAND gate 1221 is provided with a logic "1" from serial shift register 1352.

Detailed Description Text (216):
In a read sequence, receiver unit 2000 activates sensor unit 1000 with infrared read transmission carrier frequency (step 3110). The analog-to-digital conversion

will begin in sensor unit 1000. Next, receiver unit 2000 clocks out the 8 bits of data from serial shift register 1352 (step 3120). Sensor unit 1000 sends a 38 kHz carrier frequency which are detected by receiver unit 2000. Receiver unit 2000 verifies the signal from sensor unit 1000 (step 3130). If the value is verified, receiver unit 2000 stores the value (step 3140). If the signal is not verifiable, receiver unit 2000 clocks the data from sensor unit 1000 (step 3120). After the measurement is stored, the read count value is incremented (step 3150). Receiver unit 2000 ceases sending activation signals after the value is stored (step 3160). Receiver unit 2000 waits for the deactivation time to be reached. In response to the absence of activation signals for 125 milliseconds, sensor unit 1000 is turned "OFF" (step 3170).

Detailed Description Text (225):
Receiver units 2000 provide the pressure data to a large display situated so that the driver can read the display from cab 3020 of truck 3000. The display may be employed as red and green lights so that a red light is illuminated if any sensor 1000 transmits an unsafe pressure value. If all sensor units 1000 transmit safe pressure values, a green light is illuminated. This application is desirable in light of the stricter regulations regarding truck tire pressures on highways.

Detailed Description Text (229):
It will be understood that while the various conductors/connectors may be depicted in the drawings as single lines, they are not shown in a limiting sense and may comprise plural conductors/connectors as understood in the art. Further, the above description is of preferred exemplary embodiments of the present invention; the invention is not limited to the specific forms shown. For example, while sensor unit 400 has been shown, it is understood that various sensing devices could be substituted. In addition, the transducer circuit need not have an independent power source; rather, power may be delivered from the transmitter unit to the transducer unit, as desired. Further still, the invention has been described with reference to block diagrams. These function blocks can be combined into the same device or separated into different discrete devices. For instance, the entire sensor unit 400 could be implemented as one integrated chip. These and other modifications may be made in the design and arrangement of the elements discussed herein without departing from the scope of the invention as expressed in the appended claims.

CLAIMS:

1. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a display unit in remote communication with the sensor unit and being operable for selectively transmitting the command signal to the sensor unit, for receiving from the sensor unit the response signal indicative of the parameter, and for displaying information relating to the parameter.

4. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a transmitting and receiving unit in remote communication with the sensor unit and being operable for selectively transmitting the command signal to the sensor unit, for receiving from the sensor unit the response signal indicative of the parameter, and for enabling the display of information relating to the parameter.

7. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a display unit in remote communication with the sensor unit and being operable for transmitting the command signal to the sensor

unit in response to an indication from a user for a sensor reading, for receiving from the sensor unit the response signal indicative of the parameter, and for displaying information relating to the parameter.

10. A sensor and display system comprising: a sensor unit coupled to a vessel and receptive to a command signal, the sensor unit sensing a parameter of the vessel and generating a response signal indicative of the parameter in response to receiving the command signal; and a transmitting and receiving unit in remote communication with the sensor unit and being operable for selectively transmitting the command signal to the sensor unit in response to an indication from a user for a sensor reading, for receiving from the sensor unit the response signal indicative of the parameter, and for processing information conveyed in the response signal.

13. The system of claim 10, wherein the transmitting and receiving unit enables information related to the parameter to be displayed.

14. In a system comprising a sensor unit operatively coupled to a vessel and in remote communication with a receiving unit, a method for obtaining information related to a parameter of a vessel, the method comprising: receiving at the receiving unit an indication from a user to activate the sensor unit; remotely activating the sensor unit in response to receiving the indication; obtaining information related to the parameter with the sensor unit; sending a signal indicative of the parameter from the sensor unit to the receiving unit; and receiving the signal at the receiving unit.

17. A method of receiving and displaying information in a display unit, wherein the information is conveyed in a signal transmitted from a sensor unit physically separate from the display unit, the method comprising the steps of: receiving an indication from the user to activate the sensor unit; in response to receiving the indication from the user, remotely activating the sensor unit; remotely receiving the signal from the activated sensor unit; conditioning the signal for display; and displaying information conveyed in the signal.

DOCUMENT-IDENTIFIER: US 5341130 A
TITLE: Downward compatible AGV system and methods

Brief Summary Text (5):
Later U.S. Pat. Nos. 4,791,570 and 4,902,948 of this assignee describe communication systems and methods for controlling a plurality of task-performing AGV's along a network of guide wires. U.S. Pat. Nos. 4,791,570 and 4,902,948 describe a guide wire logic and communications capability which provides for infinite expansion as to the number of guide wire loops and vehicles which comprise the system; accommodates polling of vehicles of the system not at predetermined times but only upon the occurrence of certain events, causes high data transmission rates to occur over low frequency carriers using the guide wires.

Brief Summary Text (7):
U.S. Pat. No. 4,908,557 issued to Masahiro Sudara discloses a control apparatus which navigates along a path defined by update magnets arranged in the floor such that a null or bipolar signal is produced in each detecting sensor of a Hall sensor array located in each AGV. An algorithm is described which calculates position of the magnet based upon treating each sensor as a point or unit of measurement and performs calculations based upon a minimum distance in units of sensor positions. The precision of measurement is statistically dependent upon the physical displacement of each of the Hall sensors and the steepness of the signal about the transition between the magnet's North and South fields. As such, the precision of measurement of a magnet's position by the method described by Masahiro Sudara is of the order of magnitude of the center-to-center spacing of the Hall sensors. This level of measurement precision produces errors in vehicle bearing estimates which markedly restricts allowable distance of separation between the update magnets in the vehicle path, significant precision being required to provide assurance the vehicle will retain sufficient bearing accuracy to acquire to stay on a planned path between widely separated magnets.

Brief Summary Text (54):
It is another object, in one embodiment, to utilize one or more phase-locked loops to process signals received by receiving antennas in detecting a passive conductive floor loop, and in which the receiving circuits have capability for initialization and for automatic gain control of the phase-locked signal level.

Brief Summary Text (71):
It is another important object to provide a navigation and guidance system which comprises a programmed "E" stop, which is triggered by a digital processor interrupt and brings an AGV to a slow, controlled stop when an emergency stop requirement is detected.

Brief Summary Text (72):
It is another important object to provide navigation and guidance system which comprises a backup to the "E" stop which immediately halts progress of the AGV when an "E" stop malfunction is detected.

Drawing Description Text (25):

FIG. 18. Simplified diagram of wire-crossing detection circuits. (See FIG. 19 for details.)

Drawing Description Text (26):
FIG. 19. Circuit diagram of wire-crossing detection circuits including antennas (i.e., coils) and signal-combining circuits.

Drawing Description Text (27):
FIG. 20. Circuit diagram of a portion of wire-crossing detection apparatus tuned to a frequency assigned for active guidewire operation of the vehicle.

Drawing Description Text (28):
FIG. 21. Circuit diagram, a continuation of FIG. 20, of a portion of wire-crossing detection apparatus tuned to a frequency for active guidewire operation.

Drawing Description Text (29):
FIG. 22. Circuit diagram of a portion of wire-crossing detection apparatus tuned to a frequency assigned for passive wire loop operation in a terminal.

Drawing Description Text (30):
FIG. 23-27. Signal waveforms at various points in the wire-crossing detection circuit of FIG. 21, namely at terminals 253, 257, 267, 271, and 261, respectively.

Drawing Description Text (31):
FIG. 28. Block diagram of an alternative embodiment of the invention that uses phase-locked oscillators in a portion of the system for processing signals from lateral-position-detecting antennas.

Drawing Description Text (42):
FIG. 38 is a simplified flow chart of an algorithm for processing sensor data to measure the lateral position of the vehicle relative to a magnet and to detect when a row of Hall sensors crosses the magnet.

Drawing Description Text (45):
FIGS. 40A and 40B comprise a simplified flow chart of an algorithm for processing sensor data to concurrently measure the lateral position of the vehicle relative to two magnets and to detect when the row of Hall sensors crosses each magnet.

Drawing Description Text (79):
FIG. 73 is a block diagram of vehicle communications electronics showing connecting relationships among a communications processor, an SDLC chip, a radio data decoder, and a two-way radio.

Drawing Description Text (81):
FIG. 75 is a detailed schematic of the automated guided vehicle controller communications electronics which receive input from the radio data decoder, said electronics comprising an SDLC chip, a central processing unit, a clock generator, and floor controller interfacing circuits.

Detailed Description Text (16):
Base station 802 received data is detected at antenna 15 and relayed to radio 804 wherefrom, the data in audio format, is sent to radio data decoder 820 wherein the audio RxAUDIO 870 signals are transformed to RxDATA 874 signals which can be processed by SDLC chip 812. Once processed by SDLC chip 812, data is sent through bus 816 for storage in memory and further transmission to AGVC computer 13A after conversion to the selected RS422 or RS232 format.

Detailed Description Text (20):
A digital decoding circuit 1120 portion of radio data decoder 820 is seen in the circuit schematic in FIG. 74. A 9600 baud digital data stream is sent to radio 804

wherefrom the signal is modulated and sent over a carrier wave to another receiving radio 804. Using digital decoding circuit 1120, the 9600 baud stream requires a base band of only one-half the 9600 baud digital data stream frequency to send a signal which, as received and provided by a receiving radio 804, produces a discriminator waveform seen as discriminator output 1136 in FIG. 76. Digital decoding circuit 1120 receives and reconstructs the 9600 baud signal which is transmitted effectively at 4800 cycles per second. Even at 4800 cycles per second, received signal amplitude is substantially lower than other radio signals which are transmitted at frequencies lower than the 3000 cycle per second base band cutoff of radio 804. Digital decoding circuit 1120 is of primary importance in the digital data reconstruction because a frequency of 9600 cycles per second is too far beyond the 3000 cycle per second base band cutoff of radio 804 to be reliably detected. Even so, the amplitude of the 4800 cycle per second frequency signal requires special processing to reliably reconstruct the original digital data stream.

Detailed Description Text (40):
Touch-sensitive bumpers 20, 22 are located at the front and rear of the vehicle, respectively, to detect obstacles in the path and to activate switches to stop the vehicle.

Detailed Description Text (45):
Radio data decoder 820 operates as earlier described. Also as earlier described, lines RxDATA 874, RTS 840, CTS 842, and TxDATA communicate received data, request to send, clear to send, and data to be transmitted, respectively, between radio data decoder 820 and SDLC 812, over lines 818 in the directions shown. SDLC operates as is well known in the art. A bus 816 provides communication between SDLC 812 and CPU 810'. A circuit diagram which includes the circuits related to the vehicle 2A provided in FIGS. 87-95 and hereafter described as part of the vehicle 2A microprocessor system.

Detailed Description Text (53):
Touch-sensitive feelers or bumpers 20, 22 are located at the front and back of the vehicle respectively to detect obstacles in the path and to activate switches to stop the vehicle. A transversely arranged linear array of magnetic sensors 24 is mounted on the vehicle as shown in FIG. 32.

Detailed Description Text (58):
The sensors 24 are commercially available devices whose analog output voltage varies as a function of the magnetic field it detects. Each sensor has a null voltage, which is its output when no magnetic field is present. When a magnetic field is present the voltage consistently increases or decreases relative to the center of flux of a magnet and to the null voltage, depending upon whether the magnet crosses a south or north pole. In the described embodiment of the invention the sensors always detect a south pole field 31, so their output voltage always increases as a result of being near a magnet.

Detailed Description Text (63):
Output data from the microcontroller 482 are in serial form differential output at a line 484, which conducts the data through a communication chip 485 and differential output lines 481, therefrom, to a communication board, not shown. A control bus 486 enables the microcontroller 482 to control multiplexers 470, 471 and the A/D converter 478 as described more fully below.

Detailed Description Text (78):
Detection of a Magnet

Detailed Description Text (120):
The next program function, performed in block 542, is to determine whether or not the peak of sensor voltage has been passed. The peak values of output voltage from the Hall sensors of array 24 occur when the array 24 is directly over the floor-

mounted magnet 6. When the reading of the sensors start to decline the array of sensors has passed over the center of flux of magnet 6. This condition is detected by block 542 by conventional programming.

Detailed Description Text (124):
The process of selecting a group of sensors, looking up distances and averaging them is a form of cross-correlation of received signals with a stored field pattern. This result is transmitted, block 546, from the microprocessor 482 to a main microprocessor, not shown. It is transmitted promptly when the peak readings are detected, so the time of transmission of the data serves as an indication of the time at which the sensor array 24 crosses marker magnet 6. In this way both lateral and longitudinal position information are obtained from one passage of the array 24 over magnet 6.

Detailed Description Text (130):
As before described, the null offsets are calculated during a known null period as specified in blocks 522, 524, and 526. As earlier described, in FIG. 39, a WAIT LOOP 528' provides an updating of the null calibration for each of the sensors until an over threshold measurement indicates detection of magnetic flux of a first magnet 6 or 6'. Upon such detection as part of block 536 activity, the sensor values are stored and the sensor having the strongest signal is selected as earlier described for block 536 in FIG. 38. In addition in block 536, a first sensor group active flag is set to signal a first magnet position measurement is active.

Detailed Description Text (131):
As earlier described, the activities of blocks 538, 540, and 544 select the group of sensors used in the calculation of what is now the first sensor group, interpolate the distance from each sensor of the first group to the center of magnetic flux of the first detected magnet and average, then calculate a running average of the position of the vehicle relative to the magnet. Decision block 542 branches to a block 546' when the peak value of the first sensed signal is detected or to a second path headed by START 2 before the peak is discovered.

Detailed Description Text (132):
At START 2, input program flow line 622 leads to decision block 624 wherein a decision is made whether or not a second group active flag is set indicating a signal has previously been detected from a second magnet. If the second group flag is not set, a single pass through blocks 630, 632, and 634 is made. Blocks 630, 632, and 634 comprise programming functions which are similar to those described for blocks 530, 532, and 534, except blocks 630, 632, and 634 only process information related to sensors of array 24 not involved with the first group. If no threshold is detected in block 634, an updated null calibration is calculated for each sensor which is not part of the first group and a branch is made TO CONTINUE to merge with program flow line 620. If a signal above threshold is detected, a branch is made to block 636 wherein the appropriate signal values are stored and processed as in block 536 for a second group of sensors and the second group active flag is set.

Detailed Description Text (135):
From decision block 660, a branch is made to block 638 if the first group active flag is reset indicating a peak has been detected for the first measured magnetic field. If the first group active flag is set, the program proceeds to program flow line 620 whereat block 538 is entered to subsequently process the output of the first group of sensors dedicated to making a measurement of the position of the first detected magnetic field.

Detailed Description Text (136):
If within block 542 a peak voltage is detected, the programs proceeds to block 546' wherein the measured position determined by first group measurements are stored for later recovery and transmission to the main processor and the first group active

flag is reset. From block 18', decision block 654 is entered, wherein a branch is made to proceed TO START 2 through program flow line 622 if the second group active flag is set or to proceed to block 656 if the second group active flag is reset. At block 656, only the first group measured position is reported based upon only one magnetic field having been detected and no concurrent measurement having been made.

Detailed Description Text (168):
The transmitter is shown in more detail in FIG. 6. The main component of its oscillator 68' is a conventional commercially available chip 68A. Its output at terminal 68B is connected to the analog on-off switch 70. When the switch is in a conductive condition the oscillator's signal is connected to input 69A of one side of a push-pull current driver amplifier 69.

Detailed Description Text (171):
The analog on-off switch 70 is operated by a signal at a terminal 70C, which comes from the outer loop microprocessor 67. The transmitter system comprising elements 68', 69, 70 and 71 is turned off by operation of the switch 70 when the vehicle is being operated in a mode in which it follows an actively energized guidewire. The outer loop processor receives information from the AGVC 13, which keeps track of whether or not the vehicle is approaching or in a terminal.

Detailed Description Text (174):
The operation of the transmitter is as follows: The oscillator 68 produces a signal which can be connected through the analog on-off switch 70 to the push-pull drivers 69. The output signal from the push-pull drivers 69 energizes the transmitting antenna 71.

Detailed Description Text (177):
FIG. 7 also shows a receiving antenna assembly 91. It detects magnetic fields produced by currents in wires on the floor. In this preferred embodiment, a single ferrite rod core 93 is used, with one receiving coil 95 mounted near the left end of the rod and another receiving coil 97 mounted near the right end of the rod 93. Alternatively, two shorter ferrite rods can be employed with a fixed lateral space between them, each encircled by only one of the two receiving coils 95, 97.

Detailed Description Text (188):
Figures relating to hybridity include FIGS. 4 and 13. The vehicle navigation and guidance system, in the self-contained mode, operates by starting with a known position and heading and measuring the distances traveled by both the left and right sides of the vehicle. It integrates those distances to keep track of the location of the vehicle. The position is updated periodically by detecting a magnet of known position such as magnet 6 in the floor over which the vehicle travels.

Detailed Description Text (190):
The active guidewire-signal channel's error signal at terminal 169 of FIG. 16B is switched off so that it does not interfere with the passive wire loop's signal at terminals 122 and 124. This insures that the passive wire loop's signal (FIGS. 12 and 13) completely controls the vehicle. More detailed descriptions of the circuits involved are presented below.

Detailed Description Text (215):
The signal at 118 goes through a path including the motion control processor 61, (and necessary A/D and D/A converters), FIG. 13. The signal at terminal 155 is amplified in a bandpass filter 157 and then rectified (159), and no bias is removed, leaving the difference at terminal 160 very small. Consequently the error signal is very small. The signal at 169 is switched off by the outer loop processor 67 while the vehicle is traveling in over a passive guidewire, to eliminate any possible undesirable effects. (See switch 170, FIGS. 4B and 16B).

Detailed Description Text (220):
The outer loop processor 67 alternates the center frequency of this bandpass filter 157 by means of an analog switch, which switches appropriate resistor values into the circuit to select the desired frequency, until a significant amplitude is detected, signifying acquisition of the guidewire. The filtered signal is fullwave rectified in a block 159. The result at terminal 160, which is from starboard signal channel, is sent to a non-inverting input of a summing junction 161.

Detailed Description Text (238):
To summarize, the terminal-positioning mode of the vehicle navigation and guidance system apparatus guides the vehicle on a guidewire portion 3 of an installation in the following manner. The transmitter assembly 68', 69, 71 is turned off by means of the switch 70 of FIGS. 5 and 6. Signals from guidewires, received at the receiving antenna 91, are preamplifled (FIG. 15) and routed directly to an analog circuit board (FIG. 14). The starboard and port signals C.sub.s (n) and C.sub.p (n) above replicate, with opposite signs, the commands being received at terminals 122 and 124 from the microprocessor 61. The summing junctions 175 and 177 output speed commands, varied slightly by error signals, to control the motors 15 and 17 to drive the vehicle.

Detailed Description Text (242):
Wire-Crossing Detection for Longitudinal Positioning of Vehicles

Detailed Description Text (246):
When the coil 207 is directly over the current-carrying floor wire, an alternating magnetic flux would therefore produce one phase of signal in the coil 205, an opposite phase of signal in the coil 209, and zero signal in the coil 207. The principle of operation of the apparatus in detecting the longitudinal location of the vehicle by means of wire-crossing detection based on these three signals.

Detailed Description Text (254):
The logic circuit involving NAND gate 221 and circuits leading up to it are arranged so that when the signal at 220 is crossing zero and the signal at 227 is relatively great (although not necessarily a maximum) the NAND gate 221 outputs a logic signal at the point 229 that is suitable for indicating that the vehicle is directly over the wire crossing. That output at 229 is low when a wire crossing is detected.

Detailed Description Text (258):
The output of summing inverting amplifier 225 is at terminal 241, which is shown on both FIG. 19 and FIG. 20. The signal at terminal 235 is the wire-crossing signal itself and that at 241 is the reference wire-crossing signal. The circuits of FIG. 19 are used in common to detect wire crossings that are (a) directly energized as in terminal 9 of guidewire routes 3, and (b) passive induction loops as at terminal 11.

Detailed Description Text (260):
The two frequencies 965 Hz of FIG. 20 and 1155 Hz of FIG. 22 are used in a guidewire system for causing the vehicle to branch to a first or second route at a junction such as a "T", by applying an appropriate frequency to the guidewire when the vehicle approaches the junction. However, in a terminal having a passive loop, the receiver subchannel of 1155 Hz frequency is used for detecting a passive loop signal, whose energy originated with the onboard transmitter 68, and the receiver subchannel of 965 Hz frequency is used for detecting a conductively energized active guidewire crosswire at the terminal.

Detailed Description Text (261):
Thus the 1155 Hz passive-wire-crossing subchannel 277 (see FIG. 4), is used for detecting a passive loop when the vehicle is in a terminal, and is used for detecting a junction guidewire when the vehicle is not in a terminal. The 965 Hz

guidewire-crossing subchannel 243 of FIG. 4 is dedicated to only guidewire sensing, both in and out of terminals.

Detailed Description Text (262):
On FIG. 20, the signal of terminal 235 passes through switching to a bandpass filter 245. FIG. 21 is a continuation, at terminals 246 and 248, of FIG. 20. The output of filter 245 passes through an amplifier circuit 247, a switch 249, and an inverting amplifier 251. The output of inverter 251 is shown in the graph of FIG. 23. That graph is the detected wire-crossing signal at a terminal 253.

Detailed Description Text (269):
The curves of FIGS. 23 through 27 are aligned vertically over each other to provide the same vehicle-position scale on the abscissa for all of them. Collectively they portray what happens in the circuit when a guided vehicle having antennas 205-215 as in FIG. 7 enters a terminal and drives over a wire-crossing that it must detect for purposes of longitudinally positioning the vehicle. The abscissa of all of the graphs of FIGS. 23 through 27 is distance expressed in inches, as measured positively and negatively from a zero point 283 on FIG. 23. Point 283 is the vehicle's position when the middle coil 207 is directly over the wire-crossing on the floor.

Detailed Description Text (302):
Terminal 369 is connected to a voltage-controlled digital oscillator 370; it produces output pulses at a frequency that depends upon the control voltage at terminal 369. The oscillator 370 provides output pulses at a terminal 364, which are conducted to the clock input terminal of the counter 372. The oscillator 370 is a model NE555, manufactured commercially by Texas Instruments, Inc., Dallas, Tex., 75265.

Detailed Description Text (308):
The frequency of pulses at the clock input terminal of the counter 372 depends inversely upon the magnitude of the voltage at terminal 362; a greater magnitude results in a greater frequency of the pulses that are counted by the counter 372. Consequently the offset calibration signal at terminal 361 approaches a final value faster when it has farther to go. It reaches a final value when the voltage at terminal 362 is zero, which reduces the counting rate at terminal 364 to zero. The counter 372 retains its count contents, so the proper bias voltage remains on the bias terminal 361.

Detailed Description Text (319):
A package 901 (see FIG. 61) comprising heaters and insulators completely encompass angular rate sensor 900 and is affixed to support 992 which is shock mounted to inertial table 700 with stand-offs 912. On the opposite side of inertial table 700, printed circuit board 904 is firmly affixed in vertical orientation. A shaft is centrally disposed through and connected to moving parts of the gyro 500 comprising slip ring assembly 906, a hub 994 which firmly supports inertial table 700, a motor rotor 922 (seen in FIG. 60), and the moving parts of encoder 88'. Wires and other parts, such as circuit component details and power supply parts are not shown for clarity of presentation.

Detailed Description Text (321):
A block diagram of the gyro 500 is seen in FIG. 63. A signal comprising the rate of angular change is sent to a network of amplification and compensation circuits 998 wherefrom feedback current to drive motor 916 is provided. Motor 916 is driven to maintain angular rate sensor 900 in a null direction. The angular travel of motor 916 is sensed by encoder 88' wherefrom a signal is provided to outerloop processor 67 for Kalman filtering and other processing.

Detailed Description Text (325):
The selected angular rate sensor 900 is an entirely solid state, "tuning fork",

single axis sensor and utilizes piezoelectric vibrating beam technology to produce an inertial sensor with no moving parts. It provides an analog output voltage which is proportional to the angular rate about its sensing axis. At zero angular rate, the output is zero volts. Full scale angular rates produce an output of +10 or -10 volts, dependent upon direction of rotation. A dual power supply, providing regulated +15 and -15 volts, is required.

Detailed Description Text (329):
The output of function 986 is fedback through gain K.sub.e to summer 980. In addition output of function 986 (.omega..tau.) feeds back to summer 968, providing angular table error rate .omega..sub.e. Further, output of function 986 is detected by an encoder 88' (see FIG. 63) and fed to a direction and integration circuit 90 which provides input to outerloop processor 67, as seen in FIG. 56.

Detailed Description Text (394):
The Kalman filter loop time is variable and is designated T.sub.k. In the currently preferred embodiment, a Kalman filter cycle occurs immediately after the detection of a marker 6, at which time an observation is made of vehicle azimuth angle differences (table 700 vs. wheel 57, 59 data) and upon initial insertion of manual azimuth angle into the system. Each observation is assumed to be independent of the others (down-range vs. cross-range in the vehicle frame because of their orthogonality). Thus, the Kalman filter will process marker observations (sequentially) and angle comparisons concurrently.

Detailed Description Text (489):
.delta.z=detected-calculated measurements

Detailed Description Text (491):
The "preferred embodiment" involves also taking an azimuth measurement at the time the magnet is detected to provide overlapping, redundant information.

Detailed Description Text (527):
Analog input processor 1170 provides analog to digital input processing, wherein analog voltage inputs from each tachometer 33, see FIG. 4A, are received, digitized, and monitored, thereby providing a safety backup to operation of motion control processor 61. In addition, analog input processor 1170 receives and processes inputs from a joy stick on a manual vehicle control box whereby each vehicle 2A is manually controllable. Further, analog input processor 1170 receives and processes inputs from obstacle detectors and AGV 2A battery voltage. Analog input processor 1170 is an 8742, available from Intel Corporation.

Detailed Description Text (528):
Motion control processor 61 function and responsibility are described in detail earlier. As seen in FIG. 77, motion control processor 61 receives inputs from encoders 58 as earlier described and provides digital to analog outputs which control operation of drive wheels 8, 10. Motion control processor 61 also provides a controlled "E" stop to bring AGV 2A to rest in a rapid, but not hard-braking stop in a detected emergency. Motion control processor 61 is preferably a DS5000 central processing unit, available from Dallas Semiconductor. A second, more direct, but gated signal path 1184, 1162, 1186 provides direct feedback from analog input processor 1170 to motion control processor 61.

Detailed Description Text (529):
In the currently preferred embodiment, output processor 1166, encoder processor 1164, analog input processor 1170, gated interface 1162 between analog input processor and motion control processor 61, motion control processor 61, and input processor 61 are installed on a single digital I/O board 1194. Detailed circuit schematics and layout orientation of digital I/O board 1194 are provided for completeness of disclosure in FIGS. 86-95. FIG. 86 provides a map showing relative orientation of FIGS. 92 and 93. All components seen in the above referenced figures

are commercially available and are used in a manner which is known in the art. Power supply interconnections are removed for clarity of presentation. A list of component types and values, where applicable, for digital I/O board 1194 is found in the following table.

Detailed Description Text (530):
Two central processing units are installed on the vehicle 2A communications board 824. As seen FIG. 77, communications board 824 comprises serial I/O communications processor 1192, SDLC communications processor 810', SDLC chip 812, and radio data recorder 820, and all related interfacing logic and other components.

Detailed Description Text (533):
Detailed schematics of communications board 824 are seen in FIGS. 78-85B. All components are commercially available and are used in a manner which is known and in the art. Note that some earlier disclosed circuits are repeated therein. For example, FIG. 85 comprises components and circuits found in radio data recorder 820, earlier seen in FIG. 74. Power supply interconnections are removed for clarity of presentation. A list of component types and values, where appropriate, for communications board 824 is found in the following table.

CLAIMS:

6. A downwardly compatible automated guided vehicle system according to claim 1 wherein the at least one automatic guided vehicle comprises two-way wireless vehicle communications means.

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L18: Entry 3 of 4 File: USPT Aug 23, 1994

US-PAT-NO: 5341130
DOCUMENT-IDENTIFIER: US 5341130 A

TITLE: Downward compatible AGV system and methods

DATE-ISSUED: August 23, 1994

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APPL-NO: 07/ 908691 [PALM]
DATE FILED: June 26, 1992

PARENT-CASE:
This application is a division of our co-pending U.S. patent application Ser. No. 621,486, filed Dec. 3, 1990, now U.S. Pat. No. 5,281,901, which issued Jan. 25, 1994.

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FIELD-OF-SEARCH: 340/825.06, 180/168, 318/587, 364/424.02

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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ART-UNIT: 264

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ABSTRACT:

An automated guided vehicle (AGV) control system which is downward compatible with existing guidewire systems providing both guidewire navigation and communication and autonomous navigation and guidance and wireless communication between a central controller and each vehicle. Vehicle steering and control includes autonomous guidance and navigation of the vehicle over paths marked by update markers which may be spaced well apart, such as fifty feet. The control system employs high

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frequency two-way data transmission and reception capability over the guidewires and via wireless communications. The same data rates and message formats are used in both guidewire and wireless communications systems. Substantially the same communications electronics are used for the central controller and each vehicle. Novel navigation and guidance algorithms are used to select and calculate a non-linear path to each next vehicle waypoint when the vehicle is operating in the autonomous mode. The non-linear path orginates with an initial direction equal to the heading of the vehicle as it enters the path and a waypoint heading defined as part of the message received from the central control system which plans and controls travel of each vehicle in the system.

37 Claims, 134 Drawing figures

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L10: Entry 22 of 22 File: USPT Sep 19, 1978

US-PAT-NO: 4114730
DOCUMENT-IDENTIFIER: US 4114730 A
**** See image for Certificate of Correction ****

TITLE: Transportation system with individual programmable vehicle processors

DATE-ISSUED: September 19, 1978

INVENTOR-INFORMATION:

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NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Reliance Electric Company	Cleveland	OH			02

APPL-NO: 05/ 721062 [PALM]
DATE FILED: September 7, 1976

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US-CL-ISSUED: 187/29R
US-CL-CURRENT: 187/247

FIELD-OF-SEARCH: 187/29

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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ART-UNIT: 217

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ABSTRACT:

A transportation system, illustrated as an elevator system, including a programmable processor for controlling the operation of the elevator car. The processor generates all the control signals to an elevator control means in response to the reception of service condition signals representing data on the status of the elevator system components. Where two or more elevator cars are grouped together for servicing a plurality of common stations, each car has an associated processor and one processor is designated as the master processor. The master processor is programmed to assign the hall calls at the stations to its associated elevator car or to a selected one of the various other elevator cars through their processors designated as slave processors. Each processor reads the service condition signals for its associated car such as calls from passengers within the car, vehicle position signals, the status of its prime mover, the assignment of a car to receive passengers queued up at a given station, and whether or not the car doors are closed and generates the control signals in response thereto in accordance with a predetermined program.

53 Claims, 41 Drawing figures

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Abstract Text (1):
A transportation system, illustrated as an elevator system, including a programmable processor for controlling the operation of the elevator car. The processor generates all the control signals to an elevator control means in response to the reception of service condition signals representing data on the status of the elevator system components. Where two or more elevator cars are grouped together for servicing a plurality of common stations, each car has an associated processor and one processor is designated as the master processor. The master processor is programmed to assign the hall calls at the stations to its associated elevator car or to a selected one of the various other elevator cars through their processors designated as slave processors. Each processor reads the service condition signals for its associated car such as calls from passengers within the car, vehicle position signals, the status of its prime mover, the assignment of a car to receive passengers queued up at a given station, and whether or not the car doors are closed and generates the control signals in response thereto in accordance with a predetermined program.

Brief Summary Text (5):
This invention relates in general to a supervisory system for controlling the operation of a vehicle in a transportation system and, in particular, to a programmable processor for controlling a vehicle by receiving service condition signals from the control system and generating control signals in response thereto to control the vehicle in accordance with a predetermined program.

Brief Summary Text (7):
In the discussion which follows, the transportation system of the invention will be disclosed as an elevator system in which the vehicle or vehicles of the system are elevator care, the station calls registered by prospective passengers will be elevator hall calls, the calls registered by passengers within the vehicle will be elevator car calls and the various other system functions will be discussed in elevator system parlance. However, it is to be understood that the invention is applicable to other transportation systems such as horizontally traveling cars or trains of cars for mass transit systems, the class of systems employing smaller vehicles identified as personal rapid transit systems, or conveyors as employed in warehousing and local distribution systems.

Brief Summary Text (15):
The processor includes a memory for storing the program, an arithmetic logic unit for performing the calculations required by the program and a plurality of registers for manipulating data. Data representing service conditions in the elevator system is received by the interface circuits and is transmitted to the processor over the bus under the direction of the program. The processor utilizes the data to generate control signals which are transmitted over the bus to the interface circuits to control the various elements of the elevator system.

Drawing Description Text (11):
FIG. 10 is a schematic diagram of the transmitter and clock of FIG. 8;

Drawing Description Text (12):
FIG. 11 is a waveform diagram of the clock pulse trains generated by the transmitter and clock of FIG. 10;

Drawing Description Text (13):
FIG. 12 is a schematic diagram of the transmitter/receiver interface circuit of FIG. 8;

Detailed Description Text (5):
The motor control circuit 12 receives a speed pattern control signal from an elevator supervisor 15, which controls the operation of the elevator system. The elevator supervisor 15 receives system data signals representing car position, car speed, direction of travel, and target floor data. Car position data can be attained digitally as through an up/down counter activated by the rotational motion of the governor or elevator drive sheave. Pulses generated in given sequences can signify the direction of travel and displacement, conveniently in increments of 0.01 foot. Correction for missed count, false count, and cable stretch or slip can be superimposed on the count of the counter from a set of vanes at each floor which produce a binary code strobed each time a floor is passed. The target floors are generated by the elevator supervisor 15 utilizing target floor data which include hall call and car call data from a parallel input/output circuit 16. The circuit 16 receives multiplexed car call signals from the elevator car 13 and hall call signals from a pair of push buttons 17 and 18 located at the floors or landings where the elevator car 13 can stop.

Detailed Description Text (13):
The main circuit breaker 51 also protects a relay power supply 52 which is connected to the input line 48 through the breaker. The input line 48 is also connected to a raw power supply 53 which transforms the relatively high voltage input power into a relatively low voltage, typically twenty-four volts, unregulated direct current input power. The unregulated power from the raw power supply 53 is connected to a supervisor power supply 54 which supplies regulated power at various voltages to the circuit elements of an elevator supervisor 55. Typically, the supervisor power supply 54 may generate regulated direct current power at positive five volts, negative twelve volts, positive and negative fourteen volts, and positive and negative twenty-four volts.

Detailed Description Text (15):
The processor 57 includes a memory for storing a program and data and an arithmetic and logic unit for performing the calculations required by the program. Data representing service conditions in the elevator system is received by the supervisor interface circuits 58, 59 and 61 and is transmitted to the processor 57 over the bus 56. The processor 57 utilizes the data to generate control signals which are transmitted over the bus 56 to the interface circuits 58, 59 and 61 to generate the supervisory and speed pattern control signals to the various elements of the elevator system.

Detailed Description Text (27):
In summary, there is shown in FIG. 3 a block diagram of an elevator system according to the present invention. The elevator supervisor 55 includes a processor 57 which is programmed to generate supervisory control signals and speed pattern control signals to an elevator control means in response to the reception of service condition signals representing data on the status of the system components. The service condition signals are received through and the supervisory control signals and speed pattern control signals are sent through the supervisor interface circuits such as the parallel input/output circuit 58, the safety and power

input/output circuit 59 and the position-velocity circuit 51 which are connected in parallel to the bus 56. The bus 56 is made up of a plurality of address and data lines for transmitting signals between the elements of the elevator supervisor 55.

Detailed Description Text (28):
Where two or more cars are included in the system, each car is controlled by a supervisor such as the elevator supervisor 55. One of the supervisors may be disignated as the master supervisor for alloting hall calls to the cars in the system. In this case, hall call information is transmitted between the supervisors through a multi-car supervisor circuit connected to the bus in each supervisor. Each slave supervisor performs the same functions for its associated elevator car as are performed by the master supervisor except that the slave supervisor receives hall call information from the master supervisor rather than from its own hall call interface circuit such as the circuit 62 of FIG. 3.

Detailed Description Text (38):
The power line 113 is connected to a positive power supply (not shown), typically twenty-four volts direct current, in the parallel input/output circuit for each elevator supervisor which is responsive to the hall calls. In the hall call entered circuit 91 there is shown a plurality of power input lines 115, 116, 117 and 118 connected in parallel to the power line 113 for a four car system. Each power supply is isolated from the other power supplies by a diode, such as a diode 119 in the line 115, which blocks current which might flow back to its associated power supply. The ground line 114 is also connected in the circuit 91 to a ground input line 120 which is connected to the same power supplies as are the power input lines to complete the circuits.

Detailed Description Text (41):
Before the push button 112 is pressed, the power supply voltage on the lines 63 and 95 will place a "1" at the input 123-1 to generate a "0" at the output 123-4. Since the output 123-4 is connected to a base of a NPN transistor 124 through a resistor 125, the transistor 124 is turned off. A collector of the transistor 124 is connected to the hall call push button lamp signals line 65 and an emitter is connected to the ground line 114. The "0" from the inverter 123 turns off the transistor 124 to prevent current flow through the lamp 111 and the transistor 124 from the power line 113 when the push button 112 is not actuated.

Detailed Description Text (43):
When the push button 112 is pressed, the voltage on the lines 63 and 95 will fall to a relatively low magnitude near ground potential to place a "0" at the input 123-1. This "0" is blocked from the supply voltage lead 123-2 and the emitter of the transistor 126 by the diode 127. Therefore, the power supply including the transistor 126 connectes the lead 123-2 to the supply voltage on the power line 113 less the voltage drop across the transistor 126. This voltage is prevented from reaching the input 123-1 by the diode 127 so that the inverter 123 now generates a "1" at its output 123-4 to the base of the transistor 124. The collector of the transistor 124 will be near ground potential while the push button 112 is depressed so that the transistor 124 remains turned off.

Detailed Description Text (48):
Before the push button 112, or any other similarly connected push button, is pressed, the base of the transistor 135 will be connected to the supply voltage by the resistors 134 and 136 to keep the transistor 135 turned off. Since there is no current flowing through the transistor 135, the base of the transistor 139 will be grounded through the resistor 138 to keep the transistor 139 turned off. The line 97 will be supplied with the power supply voltage from the power line 113 to represent the absence of the hall call entered signal.

Detailed Description Text (90):
The car panel (slave) multiplexer 101 is connected by the multiplexed car signals

line 64 to a transmitter/receiver interface circuit 239 in the parallel input/output circuit 58. The lobby panel (slave) demultiplexer 102 is connected to the interface circuit 239 by the multiplexed lobby signals line 103. When data is to be transmitted to the slave circuits 101 and 102, the processor generates the address bits which are received on the address lines 229 and generates the D0 data bit on one of the data lines 237. The D0 data bit is inverted to D0 by the bus interface circuit 231 and is received by the bus temporary memory 235 on a D0 line 241. The bus temporary memory 235 generates the D0 data on a XDAT line 242 to a transmitter and clock 243. The transmitter and clock 243 then multiplexes and generates the D0 data on the XA, XB transmit lines 244 to the transmitter/receiver interface circuit 239 which places the data onto the lines 64 and 103, as multiplexed output signals. The multiplexed output signals are demultiplexed by both slaves.

Detailed Description Text (91):
When data is generated as multiplexed car input signals on the line 64, the transmitter/receiver interface circuit 239 generates the data on the RA and RB receive lines 245 to a receiver 246. The receiver demultiplexes the data and generates it on a MXDI line 247 to the bus temporary memory. The processor may then address the parallel input/output circuit 58 and the bus temporary memory will generate the received data as the D0 data on the line 236 to the bus interface circuit 231 which will pass the D0 signal onto one of the data lines 237 to be read by the processor. The receiver also utilizes the MXDI signal to generate a RDAT signal. The XA transmit line 244 and the RDAT line 248 are monitored by a failure detector 249 which generates a MSOK signal to indicate a failure in the master multiplexer, the transmitter and clock 243, or generates a SLOK signal to indicate a failure in the slave multiplexer, the slaves 101 and 102. The MSOK and SLOK signal are generated on a pair of lines 250 to the data selector/multiplexer 222.

Detailed Description Text (92):
The transmitter and clock generates clock pluse trains at various predetermined frequencies, such as clock pulse trains CK0, CK1, CK2, CK3 and CK4, on a plurality of clock lines 251. These clock pluse trains synchronize the passage of data through the parallel input/output circuit 58 to enable the individual data bits to be identified as they are multiplexed, demultiplexed, placed in storage or read from storage.

Detailed Description Text (106):
FIG. 10 TRANSMITTER AND CLOCK

Detailed Description Text (108):
Referring to FIG. 10, there is shown the transmitter and clock 243 of FIG. 8 A pair of inverters 281 and 282 cooperate with a crystal 283 to generate a train of clock pulses CK having a frequency "f". The clock pulse train is divided by various denominators in a pair of counters 284 and 285 to generate the clock pulse trains CK0, CK1, CK2, CK3 and CK4 which are utilized to synchronize the elements of the parallel input/output circuit 58. The CK3 and CK4 pulse trains are also utilized to multiplex data from the bus temporary memory 235 of FIG. 8. The data is received on the XDAT line 242 and is sent out on the XA and XB transmit lines 244-1 and 244-2 respectively to the transmitter/receiver interface circuit 239 of FIG. 8.

Detailed Description Text (115):
The pulse trains from the transmitter and clock 243 are applied to various elements of the parallel input/output circuit 58. The CK0, CK2 and CK3 pulse trains are applied to the bus temporary memory on the clock lines 251-1, 251-3 and 251-4 respectively. The CK1 and CK2 pulse trains are applied to the receiver 246 on the cock lines 251-2 and 251-3. The CK2 and CK4 pulse trains are applied to the bus interface circuit 231 on the cock lines 251-3 and 251-5.

Detailed Description Text (116):

A data bit is received from the bus temporary memory 235 on the XDAT line 242 at a pair of inputs 291-1 and 292-2 of a pair of exclusive-OR elements 291 and 292. When both inputs to an exclusive-OR are receiving a "1" or a "0", a "0" will be generated at an output. When one input receives a "1" and the other input receives a "0", a "1" will be generated at the output. An input 291-2 receives the CK4 pulse train and an input 292-1 receives the CK3 pulse train such that the XDAT bit is multiplexed and transmitted through a pair of NAND elements 293 and 294 onto the XA and XB transmit lines respectively.

Detailed Description Text (117):
Looking at the CK3 and CK4 pulse trains in FIG. 11, it may be seen that first CK3 is at "1", then CK4 is at "1" and then both are at "0" before the cycle is repeated. The CK4 pulse train is applied to an input 295-1 and the CK3 pulse train is applied to an input 295-2 of a NOR 295 to generate a "0", "0" and "1" pulse train at an output 295-3 as shown in FIG. 11. This pulse train is applied to an input 296-1 of a NOR 296. Another input 296-2 receives a RCV signal on a line 297 from the bus temporary memory 235. If the receiver 246 is receiving data through the transmitter/receiver interface circuit 239, the RCV signal will be "1" to disable the NOR 296 and generate a "0" at an output 296-3. The output 296-3 is connected to a pair of inputs 293-2 and 294-1 to generate a "1" from the NANDs 293 and 294 at a pair of outputs 293-3 and 294-3. The output 293-3 is connected to the XA transmit line 244-1 and the output 294-3 is connected to the XB transmit line 244-2. Since both lines are at the same potential, no information is transmitted.

Detailed Description Text (118):
If the transmitter and clock 243 is to transmit, the bus temporary memory 235 generates a "0" on the RCV line 297 to enable the NOR 296 at the input 296-2. The NOR 296 will invert the pulse train from the NOR 295 at the output 296-3 as shown in FIG. 11. When the pulse train is at "1", the NANDs 293 and 294 will be enabled and when the pulse train is at "0", the NANDs 293 and 294 will be disabled to generate a "1". Therefore, two bits of information can be transmitted and the "1" on both transmit lines during the cycle serves to separate those two data bits from the two bits in the succeeding cycle.

Detailed Description Text (119):
The output 296-3 is connected through an inverter 298 to a RCV output line 299. When RCV = "1" or when both transmit lines are at "1", the output line 299 will be at "1" to indicate that the transmitter and clock 243 is not transmitting. The output line 299 will be at "0" when data is being transmitted. The RCV output line 299 is connected to the bus temporary memory 235.

Detailed Description Text (120):
If the XDAT signal is "1", the exclusive-OR 291 will respond to the CK4 pulse train at the input 291-2 to generate a "1", "0" and "1" pulse train at an output 291-3 to an input 293-1 of the NAND 293. The NAND 293 is enabled during the first two signals to invert them to a "0" and a "1" at the output 293-3 on the XA transmit line 244-1 as shown in FIG. 11. At the same time, the exclusive-OR 292 will respond to the CK3 pulse train at the input 292-1 to generate a "0", "1" and "1" pulse train at an output 292-3 to an input 294-2 of the NAND 294. The NAND 294 is enabled during the first two signals to invert them to a "1" and a "0" at the output 294-3 on the XB transmit line 244-2 as shown in FIG. 11. Therefore, a "1" data bit on the XDAT line 242 is multiplexed during the signal cycle generated from the CK3 and CK4 pulse trains and is sent on the XA transmit line as a "0" followed by a "1" while it is simultaneously sent on the XB transmit line as a "1" followed by a "0".

Detailed Description Text (121):
If the XDAT signal is a "0", the output from the exclusive-OR 291 will be a "0", "1" and "0" pulse train and the output from the exclusive-OR 292 will be a "1", "0" and "0" pulse train. The NAND 293 is enabled during the first two signals to generate a "1" and a "0", while the NAND 294 is enabled to generate a "0" and a

"1". Therefore, a "0" data bit on the XDAT line 242 is multiplexed during the signal cycle generated from the CK3 and CK4 pulse trains and is sent on the XA transmit line as a "1" followed by a "0" while it is simultaneously sent on the XB transmit line as a "0" followed by a "1" as shown in FIG. 11.

Detailed Description Text (122):
In summary, the transmitter and clock 243 generates various clock pulse trains CK0, CK1, CK2, CK3 and CK4 to the bus interface circuit 231, the bus temporary memory 235 and the receiver 246 to synchronize data flow in these elements of the parallel input/output circuit 58 of FIG. 8. The CK3 and CK4 pulse trains are utilized to multiplex a data bit on the XDAT line 242. The multiplexed data bit is sent as a sequential pair of signals on the XA and XB transmit lines 244-1 and 244-2 respectively. A "1" data bit on the XDAT line is sent as a "0" and "1" on the line 244-1 and at the same time as a "1" and a "0" on the line 244-2. A "0" data bit on the XDAT line is sent as a "1" and a "0" on the line 244-1 and at the same time a "0" and a "1" on the line 244-2. The two bits of information representing a data bit on the XDAT line are separated from the next two bits of information by a "1" signal on both transmit lines.

Detailed Description Text (123):
FIG. 12 TRANSMITTER/RECEIVER INTERFACE CIRCUIT

Detailed Description Text (124):
Referring to FIG. 12, there is shown a schematic diagram of the transmitter/receiver interface circuit of FIG. 8. Information bits to be transmitted are received on the XA and XB transmit lines 244-1 and 244-2 respectively from the transmitter and clock 243 of FIG. 10. The information bits are then sent on a pair of multiplexed car signals lines 64-1 and 64-2 to the car panel (slave) multiplexer 101 and on a pair of multiplexed lobby signals lines 103-1 and 103-2 to the lobby panel (slave) demultiplexer as shown in FIG. 8. Multiplexed car signals received on the lines 64 are sent to the receiver 246 on a pair of receive lines, RA receive line 245-1 and RB receive line 245-2.

Detailed Description Text (125):
The XA transmit line 244-1 is connected through a current limiting resistor 311 to a base of a PNP transistor 312. An emitter of the transistor 312 is connected to a positive polarity direct current power supply (not shown) and to one side of a capacitor 313. The other side of the capacitor 313 is connected to ground potential and the capacitor is charged to the potential of the power supply. The emitter is connected to the base through a resistor 314 to supply a base biasing voltage which turns off the transistor 312. The emitter of the transistor 312 is also connected through a resistor 315 to a parallel connected diode 316 and a capacitor 317. A cathode of the diode 316 and one side of the capacitor 317 are connected to the resistor 315 and an anode of the diode 316 and the other side of the capacitor 317 are connected to ground potential.

Detailed Description Text (128):
The XB transmit line 244-2 is connected through a current limiting resistor 334 to a base of a PNP transistor 335. An emitter of the transistor 335 is connected to the junction of the positive polarity power supply and the capacitor 313 and is connected to the base through a resistor 336 to supply a base biasing voltage which turns off the transistor 335. The emitter of the transistor 335 is also connected through a resistor 337 to a parallel connected diode 338 and capacitor 339. A cathode of the diode 338 and one side of the capacitor 339 are connected to the resistor 337 and an anode of the diode 338 and the other side of the capacitor 339 are connected to ground potential.

Detailed Description Text (130):
When no data is being transmitted, the XA and XB transmit lines are both at "1". Thus the transistors 312 and 335 remain turned off. Since the bases of the

transistors 318, 319, 341 and 342 are connected to the negative potential power supply the emitters of the transistors 318 and 319 are connected together and the emitters of the transistors 341 and 342 are connected together, the transistors 318, 319, 341 and 342 will be turned off and no signals will appear on the lines 64 or the lines 103.

Detailed Description Text (131):
If the "1" remains on the XA transmit line 244-1 and a "0" is applied to the XB transmit line 244-2, the transistor 312 will remain turned off and the transistor 335 will turn on to connect the bases of the transistors 341 and 342 to the positive polarity power supply. The transistor 341 will turn on to connect the windings 324 and 329 to the positive potential power supply through the resistor 337. This places a positive potential voltage on the emitter of the transistor 319 to turn it on and to connect the dotted ends of the windings 324 and 329 to the negative potential power supply. If the lines 64-2 and 103-2 are utilized as references, a negative potential signal will be transmitted on the lines 64 and 103 which represents the first half of a "0" data bit or the last half of a "1" data bit on the XDAT line 242 of FIG. 10.

Detailed Description Text (132):
If the "1" remains on the XB transmit line 244-2 and a "0" is applied to the XA transmit line 244-1, the transistor 335 will remain turned off and the transistor 312 will turn on to connect the bases of the transistors 318 and 319 to the positive power supply. The transistor 318 will turn on to connect the dotted ends of the windings 324 and 329 to the positive potential power supply through the resistor 315. This places a positive potential voltage on the emitter of the transistor 342 to turn it on and to connect the other ends of the windings 324 and 329 to the negative potential power supply. If the lines 64-2 and 103-2 are again utilized as references, a positive potential signal will be transmitted on the lines 64 and 103 which represents the last half of a "1" data bit or the first half of a "0" data bit on the XDAT line 242 of FIG. 10.

Detailed Description Text (136):
When there is no signal on the lines 64 and 103, both the RA and RB receive lines will be at "1". The capacitors 317 and 339 function as filters to pass any noise on the lines 64 or 103 to ground before the received signal is placed on the RA and RB receive lines. The diodes 316 and 338 prevent the RA and RB receive lines from falling below the ground potential during either the transmit or receive cycles.

Detailed Description Text (137):
In summary, the transmitter/receiver interface circuit 239 receives multiplexed data signals on the XA and XB transmit lines from the transmitter and clock 243 and sends those signals to either the car panel (slave) multiplexer 101 on the lines 64 and to the lobby panel (slave) demultiplexer 102 on the lines 103. When signals are received on the lines 64, they are generated on the RA and RB receive lines to the receiver 246.

Detailed Description Text (139):
FIG. 13 is a schematic diagram of the receiver 246 of FIG. 8. Inputs to the receiver are the multiplexed car signals from the car panel (slave) multiplexer 101 which have been passed through the transmitter/receiver interface circuit 239 and are applied to the RA receive line 245-1 and the RB receive line 245-2, the clock pulse trains CK1 on the line 251-2 and CK2 on the line 251-3 from the transmitter and clock 243, and a XMT signal on a line 351 from the bus temporary memory 235. Outputs from the receiver are the RDAT signal on the line 248 and a MXDI signal on the line 247 to the bus temporary memory. The receiver 246 demultiplexes the multiplexed car signals on the receive lines 245 and generates the demultiplexed data on the MXDI line 247.

Detailed Description Text (141):

The RB receive line 245-2 is connected to a data input 356-1 of a flip flop 356. An output 356-3 is connected to a data input 357-1 of a flip flop 357 and is also connected to an input 355-3 of the NAND 355. An output 357-3 is connected to an input 355-4 of the NAND 355. The clock inputs 353-2, 354-2, 356-2 and 357-2 are all connected to the clock line 251-3 to receive the CK2 pulse train. Each time the pulse train changes from "0" to "1", the flip flops will be clocked to shift data from the data inputs to the outputs. When no data is being received, the RA and RB receive lines will both be at "1". After two clock pulse train changes from "0" to "1", all the inputs to the NAND 355 will be at "1" to generate a "0" at an output 355-5. If multiplexed signals are being received, the RA and RB receive lines will be at opposite signal levels corresponding to the signals transmitted on the XA and XB transmit lines as discussed in connection with FIG. 10. Therefore, at least one of the inputs to the NAND 355 will be at "0" to generate a "1" at the output 355-5.

Detailed Description Text (145):
If the transmitter and clock 243 of FIG. 8 is transmitting, the XMT line 351 will receive a "1" to generate a "0" at the output 367-3 to continuously clear the flip flops and the shift registers. All of the inputs to the NAND 355 will be at "0" to generate a "1" to the inputs 362-1 and 364-2. The NORs 362 and 364 will each generate a "0" to the NOR 365 which in turn generates a "1" on the RDAT line 248. The "0" at the output 364-3 is applied to the MXDI line 247.

Detailed Description Text (147):
If we assume that the multiplexed signals on the RA and RB receive lines 245 are coded the same as the multiplexed signals on the XA and XB transmit lines 244, then the receiver 246 will generate the decoded multiplexed signals on the MXDI line 247. A multiplexed "1" will be received as a "0" portion on the line 245-1 and a "1" portion on the line 245-2 followed by a "1" portion on the line 245-1 and a "0" portion on the line 245-2. A multiplexed "0" will be received in the opposite order and a pause between coded signals will be received as a "1" portion on both of the receive lines 245.

Detailed Description Text (153):
Referring to FIG. 14, there is shown a schematic diagram of the failure detector 249 of FIG. 8. The RDAT signal on the line 248 and the XA signal on the line 244-1 are monitored by the failure detector which generates a SLOK signal on a line 250-1 if there is a failure of the slave multiplexer 101 and a MSOK signal on a line 250-2 if there is a failure of the transmitter and clock 243.

Detailed Description Text (156):
The XA transmit line 244-1 is connected to an input 377-1 of a monostable multivibrator 377. A second input 377-2 and a clear input 377-5 are connected to the positive polarity power supply (not shown) through the resistor 372. A non-inverting output 377-3 is connected to the MSOK line 250-2 and a cathode of a LED 378. A capacitor 379 is connected between a pair of timing inputs 377-6 and 377-7 and a resistor 381 is connected between the input 377-7 and the positive polarity power supply. An anode of the LED 378 is connected to the junction of the resistor 381 and the power supply through a resistor 382.

Detailed Description Text (157):
During each multiplexed signal on the XA transmit line 244-1, a "0" is generated to trigger the multivibrator 377. If the time between the "0" signals is less than the timing duration of the multivibrator 377, the "1" at the output 377-3 will be continuously generated to maintain the LED 378 in the off state during the operation of the transmitter and clock. If there is a failure in the multiplexer of the transmitter and clock, the multivibrator will time out and the output 377-3 will change to "0" allowing current flow through the LED 378 to light it to indicate a failure.

Detailed Description Text (180):
FIG. 16 is a schematic diagram of the bus temporary memory 235 of FIG. 8. Inputs to the memory are the A0 through A6 and A8 address signals on the output lines 393, the enable write EW signal on the line 394, the bus read BUSR signal on the line 395 and the bus write BUSW signal on the line 396 from the bus interface circuit 231; the CK0, CK2, CK3 and CK4 clock pulse trains, the read data RDAT signal on the line 248 and the multiplexed data in signal on the line 247 from the receiver 246; the RCV OUTPUT signal on the line 299 from the transmitter and clock 243; and the W1 through W4 output signals on the lines 234 from the data selector/multiplexers 222, 224, 226 and 228 respectively. Outputs from the memory are the D0 data signal on the line 236 to the bus interface circuit 231; the transmit XMT signal on the line 351 to the receiver 246; and the XDAT signal on the line 242 and the RCV signal on the line 297 to the transmitter and clock 243.

Detailed Description Text (191):
The output 454-6 is connected through an inverter 457 to a clear input 458-5 of a D-type flip flop 458 and to the reset inputs of the counters 455 and 456. Assuming that all of the counters have been reset to zero, an output 456-5 of the counter 456 is connected to a data input 458-1 of the flip flop 458 to supply a "0". The CK0 clock pulse train line 251-1 is connected to a clock input 458-2 to clock a "0" onto a non-inverting output 458-3 and a "1" onto an inverting output 458-4. The output 458-3 is connected to the RCV line 297 and the output 458-4 is connected to the XMT line 351. The "1" on the XMT line 351 enables the transmitter and clock 243 of FIG. 10 to code the data signals on the XDAT line 242 and transmit them to the car panel (slave) multiplexer and the lobby panel (slave) demultiplexer. Each coded bit that is transmitted generates a "0" pulse on the RCV OUTPUT line 299 which is connected to an input 459-1 of a NAND 459.

Detailed Description Text (192):
When the XMT signal is "1", the receiver 246 of FIG. 8 will generate a "1" on the RDAT line 248 which is connected to an input 459-2. The "0" RCV OUTPUT pulses are inverted by the NAND 459 to "1" pulses at an output 459-3 which is connected to an input 455-1 of the counter 455. The counter 455 has an output 455-6 connected to an input 456-1 of the counter 456. The frequency of the RCV OUTPUT pulse train is divided by one hundred twenty-eight at the output 456-5 which is connected to the data input 458-1 of the flip flop. The output 456-5 will remain at "0" as sixty-four coded bits are transmitted and then will change to "1". Then flip flop 458 will reverse the signals at its outputs to generate a XMT = "0" signal to stop the transmitter and a RCV = "1" signal to start the receiver.

Detailed Description Text (194):
During the transmisson of the coded bits by the transmitter, the data bits are read from the RAM 441 in multiplexed form and are generated on the XDAT line 242. When the XMT signal at the output 458-4 changes to "1", it is applied to a pair of clear inputs 462-5 and 463-5 of a pair of D-type flip flops 462 and 463. The output 441-11 of the RAM 441 is connected to a data input 462-1 and the CKO clock pulse train line 251-1 is connected to a clock input 462-2. As may be seen in FIG. 11, the flip flop will be clocked by the CKO pulse train twice during each cycle of the CK2 pulse train, once when CK2 = "1" and once when CK2 = "0". Each time the flip flop 462 is clocked, the data bit at the output 444-11 will be placed on a non-inverting output 462-3, which is connected to a data input 463-1 of the flip flop 463. The CK3 clock pulse train line 251-4 is connected to a clock input 463-2. The CK3 clock pulse train will clock the output signal at the output 462-3 onto an output 463-3 once for every twelve cycles of the CK2 pulse train. Since the RDAT signal on the line 248 also cycles once for every twelve cycles of the CK2 pulse train, the counters 455 and 456 will increment the address at the "B" inputs to the data selector/multiplexers 442 and 443 to select a different storage position.

Detailed Description Text (197):
An inverting output 465-4 of a D-type flip flop 465 is connected to an input 464-2

of the NAND 464. A data input 465-1 is connected to ground potential to supply a "0" and a clock input 465-2 is connected to the output 458-4 to receive the XMT signal. When the XMT signal changes from "0" to "1", the flip flop 465 is clocked to generate a "1" at the output 465-4 to enable the NAND 464 to pass the inverted MXDI signal. If the car panel (slave) multiplexer transmits a binary coded "0" representing the presence of a particular car signal, the receiver 246 of FIG. 13 will generate a "1" on the MXDI line which is changed to a "0" by the NAND 464. The "0" is applied to the write enable input 441-9 to write the "1" at the input 441-10 into the selected storage position. If the car signal is not present, the receiver will maintain the MXDI line at "0". The NAND 464 will place a "1" at the write enable input 441-9 and no data will be written into the RAM 441. Therefore, the received data bits are witten into the RAM 441 if they represent the presence of a car signal. The address input signals to the RAM 441 from the "B" inputs of the data selector/multiplexers 442 and 443 will be incremented in synchronizm with the MXDI signal to place that input data into the correct storage positions.

Detailed Description Text (201):
In summary, the bus temporary memory 235 stores those data bits which are to be transmitted to the car panel (slave) multiplexer and the lobby panel (slave) demultiplexer or are to be placed on the bus for the processor to read. The memory 235 includes a RAM 441 which stores the data bits. Circuitry in the memory 235 is responsive to clock pulse trains from the transmitter and clock of FIG. 10 to generate a RCV signal on the line 297 to enable the receiver to decoder sixty-four data bits from the car panel (slave) multiplexer. The decoded data bits are received on the MXDI line 247 and, if they represent the presence of a car signal, they are written into RAM 441 at a storage position determined by an address generated by a pair of counters 455 and 456. The address is incremented once for each data bit and is synchronized with the MXDI signal by the clock pulse trains.

Detailed Description Text (203):
After sixty-four data bits have been received, the XMT signal is generated on the line 351 to enable transmitter and clock to transmit sixty-four bits of data. The counters 455 and 456 will again supply the incremented address signals so that data bits read from the RAM 441 are read onto the XDAT line 242 in multiplexed form.

Detailed Description Text (211):
The transmitter and clock 243 and the receiver 246 alternate transmitting signals to the car panel (slave) multiplexer 101 and the lobby panel (slave) demultiplexer 102 and receiving signals from the car panel (slave) multiplexer 101 through a transmitter/receiver interface circuit 239. A failure detector 249 monitors the transmitter output and the receiver input and generates a failure signal on a line 250 if either the transmitter and clock 243 or the car panel (slave) multiplexer fails. The failure signal is an input to the data selector/multiplexer 222 where it is read by the processor for the further action.

Detailed Description Text (212):
The bus temporary memory stores the data bits which are sent on the XDAT line 242 to the transmitter and clock 243 to be transmitted on the lines 64 and 103 to the car panel (slave) multiplexer 101 and the lobby panel (slave) demultiplexer 102. The data bits which are received by the receiver 246 are generated on the MXDI line 247 to the bus temporary memory 235 to update the data bits in storage. The processor can change the data bits in storage by sending the address of the storage position and the new data bit through the bus interface circuit 231 and can read any data bit in storage by addressing the storage position through the bus interface circuit. Therefore, the parallel input/output circuit 58 functions as a temporary storage for the car panel and lobby panel signals.

Detailed Description Text (228):
There are ten basic instructions which may be modified to expand the capability of the processor. These instructions are: LOAD -- which directs the processor to read

data from the bus and carries its own address for the destination of the data; LOAD INDEXED -- which directs the processor to read a list of data from the bus and requires that the destination address be obtained from the file; LOAD IMMEDIATE -- which directs the processor to read a constant; STORE -- which directs the processor to place data on the bus; STORED INDEXED -- which directs the processor to place a list of data on the bus; ALU OPERATION -- which directs the processor to perform one of the ALU functions; JUMP -- which directs the processor to branch to another point in the program; CALL -- which directs the processor to branch to another point in the program and return when it is finished; TRAP -- which directs the processor to return from a CALL instruction; INC/DEC -- which directs the processor to increase or decrease the contents of a register by one; and FLAG -- which directs the processor to set or clear a set of internal flag signals.

Detailed Description Text (230):
Each instruction begins in the F1 state with the M0 clock signal. One of the registers in the file register (FR) 502 is designated as the position counter (PC) and is utilized to remember the address of the present position in the stored program. Since each instruction represents one or more steps in the program, the sixteen bit word of address information stored in the PC is sent through the multiplexer (MUX) 503 to the A register (AR) 507. The control signals for the arithmetic logic unit (ALU) 501 are generated by the extended control (XC) 512 to cause the ALU 501 to read the word from the AR 507, increment the word by one and place the word back into the PC of the FR 502. Also during the F1 state a DIP data input signal is generated by the control (C) 511 to the bus 56 to enable data on the bus 56 to be read by the processor. A first eight bit byte of data is read from the BUS and into the instruction register (IR) 506 through the bus interface (BI) 504 and the bus latch temporary (BLT) 505. This data is a binary coded representative of the instruction which is utilized to generate the instruction register signals from the IR 506 to determine which one or more of the F2, F3 and X states are to be generated and what function will be performed by the ALU 501.

Detailed Description Text (243):
FIGS. 21, 22 and 23 are schematic diagrams of the bus interface (BI) circuit 504 of FIGS. 17 and 18. All address and data signals transmitted between the processor 57 and the other circuits of the supervisor must pass through the bus interface.

Detailed Description Text (268):
All the address data and control signals which are transmitted between the processor and the other circuits of the elevator supervisor pass through the bus interface (BI) 504. FIG. 21 shows the address portion of the BI 504 which receives the AT0 through AT13 A register output signals and generates the A0 through A13 bus address signals or certain internal signals. The bus address signals may be generated only during the F1, F2 or F3 states of the processor for any instruction and druing the X state for a load or store instruction.

Detailed Description Text (362):
A clock input 916-2 is connected to an output 915-3 of an OR 915 which has an input 915-1 connected to the output 921-3 of the NAND 921. The NAND 921 may generate a "0" as was previously described to enable the OR 915. An input 915-2 is connected to an output 937-8 of a four line to ten line decoder 937. The IR0 through IR2 lines 506-1 through 506-3 are connected to a plurality of inputs 937-11 through 937-13 respectively. An input 937-14 is connected to an output 936-3 of a NAND 936 having an input 936-1 connected to the output 929-3 and an input 936-2 connected to the M1CLK line 533-6. If the AND 929 generates a "1" as was previously described and the M1CLK signal is at "1", the NAND 936 will generate a "0". If the IR0 through IR2 signals are at "1", a "0" will be generated at the output 937-8. When either or both inputs to the NAND 936 change to "0", the output 937-8 will change from "0" to "1". The transition from "0" to "1" is transmitted through the OR 915 to clock the flip flop 916 which generates the inverted BD7 signal at a non-inverting output 916-3 as the HALT signal on the line 535-1. The BD7 signal is

generated at an inverting output 916-4 as the HALT signal on the line 535-2. The output 916-4 is connected to a pair of inputs 917-1 and 917-2 of a NAND 917 to generate the inverse of the HALT signal at an output 917-3 as the PROCR signal on the line 535-3 to the bus.

Detailed Description Text (365):
A clock input 923-2 is connected to an output 922-3 of an OR 922 having an input 922-1 connected to the output 921-3 of the NAND 921 which may generate an enabling "0" as was previously described. Another input 922-2 is connected to an output 937-7 of the decoder 937. If the IRO signal is at "0", the IR1 and IR2 signals are at "1" and the output of the NAND 936 changes from "0" to "1", a "0" to "1" transition is generated at the output 937-7 which is transmitted through the OR 922 to clock the flip flop 923. The flip flop 923 will then generate the inverted BD6 signal at a non-inverting output 923-3 as the FL6 signal on the line 535-4. A clear input 923-5 is connected to the INIT line 532-4 such that a "1" to "0" transition will set FL6= "0". A preset input 923-6 is connected to a positive potential direct current power supply so that the flip flop 923 cannot be preset.

Detailed Description Text (367):
A clock input 928-2 is connected to an output 927-3 of an OR 927 having an input 927-1 connected to an output 921-3 of the NAND 921. Another input 927-2 is connected to an output 937-6 of the decoder 937. If IR1 is at "0", IR0 and IR2 are at "1", and the output 936-3 changes from "0" to "1", a "0" to "1" transition is generated at the output 937-6 which is transmitted through the OR 927 to clock the flip flop 928 if the NAND 921 generates a "0" as was previously discussed. The flip flop 928 will then generate the inverted BD5 signal at a non-inverting output 928-3 as the FB1 signal on the line 535-5 and the BD5 signal at an inverting output 928-4 as the FB1 signal on the line 535-6.

Detailed Description Text (383):
The distributed arbitrator of FIG. 36 divides requests for the bus into two groups: the first request to occur, and all other requests. All the devices are connected in series or a chain so that if two or more requests occur simultaneously, the one nearest the head of the chain will be deemed to have occurred first. Once a first request has occurred, each distributed arbitrator assumes one of two states, requesting information or transmitting information. Each device in the transmitting state, beginning at the head of the chain, generates a bus grant out (BGO) signal to the next distributed arbitrator which receives that signal as a bus grant in (BGI) signal. The first distributed arbitrator in the requesting information state will inhibit its bus grant out (BGO) signal and when the bus is free, represented by a bus busy (BB) signal at "0", that distributed arbitrator will assume control of the bus.

Detailed Description Text (389):
Assume now that the processor generates a REQBUS = "1" signal on the line 533-4. The output 977-4 of the flip flop 977 is connected to an input 965-2 to supply a "1". With both inputs at "1", the NAND 965 generates a "0" at the input 967-1 and since the input 967-2 is also at "0" from the output 968-3, the NOR 967 will generate a "1" at the input 966-2. The output 977-4 is also connected to an input 966-1 to supply a "1" and since both inputs are at "1", the BR signal will change from "1" to "0". This BR = "0" signal is applied to the BR input/output line for each device connected to the bus. The distributed arbitrator for the first device in the chain will have the BR = "0" signal applied to an input of its NOR flip flop similar to the input 968-2. Assuming that it has not received a REQBUS signal from its associated device, the NOR similar to the NOR 968 will generate a "1" to enable a NAND similar to the NAND 969. The NAND 969 has an input 969-2 connected to the BGI bus grant in line 56-2 which is connected to the BGO bus grant out line of the preceding distributed arbitrator. Since the first distributed arbitrator does not have a BGI bus grant in line, the input similar to the input 969-2 is connected to a positive polarity direct current power supply (not shown) through a resistor such

as a resistor 970 to receive a "1" to generate a "0" at an output similar to the output 969-3. The "0" is inverted to a "1" BGO bus grant out signal which is received by the distributed arbitrator in the chain. The BR = "0" signal will set each distributed arbitrator in the chain into the transmitting state when the bus grant signal is received.

Detailed Description Text (400):
The clock (CK) 533 includes a crystal controlled oscillator which generates a basic frequency which is divided to obtain the clock signals. A pair of inverters 1001 and 1002 cooperate with a crystal 1000 to generate a train of clock pulses having a frequency "F" as shown in FIG. 37. The crystal 1000 has one lead connected to an input of the inverter 1001 and the other lead connected to an output of the inverter 1002. A resistor 1003 is connected between the input and an output of the inverter 1001 and a resistor 1004 is connected between an input and the output of the inverter 1002. A capacitor 1005 is connected between the output of the inverter 1001 and the input of the inverter 1002. Another capacitor 1006 is connected between the input to the inverter 1001 and the circuit ground potential.

Detailed Description Text (404):
The output 1007-3 is connected to a pair of inputs 1009-1 and 1011-1 of a pair of NORs 1009 and 1011 respectively. The output from the oscillator is connected to a clock input 1008-1 of a J-K flip flop 1009. A J input 1008-2, a K input 1008-3 and a preset input 1008-7 are connected to a positive polarity direct current power supply (not shown) to receive a "1". A clear 1008-6 is connected to the output 1017-3 to receive a "1" to enable the flip flop. The basic clock frequency at the clock input 1008-1 is divided by two at a non-inverting output 1008-4 and is inverted and divided by two at an inverting output 1008-5. The output 1008-4 is connected to an input 1009-2 of the NOR 1009 and the output 1008-5 is connected to an input 1011-2 of the NOR 1011. Since the NORs 1009 and 1011 will only generate a "1" if both inputs are at "0", the signal at an output 1009-3 will comprise a "1" pulse followed by three "0" pulses wherein the "1" pulse occurs at the same time as the first and each subsequent odd numbered "1" pulse in the basic clock pulse train. The signal at an output 1011-13 will also comprise a "1" pulse followed by three "0" pulses wherein the "1" pulse occurs at the same time as the second and each subsequent even numbered pulse in the basic clock pulse train. The output 1011-3 is connected to the line 533-3 to generate the MCLK clock signal which has a frequency of "F/2". The output 1009-3 is connected to an input 1012-2 of a NAND 1012 and the output 1011-3 is connected to an input 1013-2 of a NAND 1013. A pair of inputs 1012-1 and 1013-1 are connected to the M0 clock signal line 533-8 to generate the M00CLK clock signal at an output 1012-3 connected to the line 533-1 and the M0CLK clock signal at an output 1013-3 connected to the line 533-2. The M00CLK clock signal is a "1" interrupted by a "0" pulse occurring at the first "1" pulse of the basic pulse train and every sixth "1" pulse thereafter with a frequency of "F/6". The M0CLK clock signal is a "1" interrupted by a "0" pulse occurring at the second "1" pulse of the basic pulse train and every sixth "1" pulse thereafter with a frequency of "F/6". The M00CLK, M0CLK and MCLK clock signals are shown in FIG. 37.

Detailed Description Text (405):
The output 1011-3 is also connected to an input 1021-1 of a NAND 1021 having another input 1021-2 connected to the M1 clock signal line 533-9 to receive the M1 clock signal. The NAND 1021 generates the M1CLK clock signal at an output 1021-3 connected to the line 533-5. The M1CLK pulse signal is a "1" interrupted by a "0" pulse at the fourth "1" pulse of the basic pulse train and every sixth "1" pulse thereafter with a frequency of "F/6". The output 1021-3 is connected to the line 533-6 through an inverter 1022 to generate the M1CLK clock signal. The M1CLK signal is a "0" interrupted by a "1" pulse at the fourth "1" pulse of the basic pulse train and every sixth "1" pulse thereafter with a frequency of "F/6". The M1CLK and M1CLK clock signals are shown in FIG. 37.

Detailed Description Text (406):
The output 1011-3 is also connected to an output 1031-1 of a NAND 1031 having another input 1031-2 connected to the M2 clock signal line 533-10 to receive the M2 clock signal. The NAND 1031 generates the M2CLK clock signal at an output 1031-3 connected to the line 533-14. The M2CLK pulse signal is at "1" interrupted by a "0" pulse at the sixth "1" pulse of the basic pulse train and every sixth "1" pulse thereafter with a frequency of "F/6". The ouput 1031-3 is connected to the line 533-15 through an inverter 1032 to generate the M2CLK clock signal. The M2CLK signal is a "0" interrupted by "1" pulse at the sixth "1" pulse of the basic pulse train and ever sixth "1" pulse thereafter with a frequency of "F/6". The M2CLK and M2CLK clock signals are shown in FIG. 37.

Detailed Description Text (450):
Now the master processor generates two sets of D0 through D7 data bits representing a hall call data address to a latch 1119. The processor also generates the address bits A0 through A13 and the DOP signal to the address decoder 1113 which responds by generating an enable signal to the latch 1119. The latch 1119 responds to each of the two sets and the enable signal to generate the A0 through A13 address bits on the lines 1121 to the bi-directional lines 76 and 77. The address bits are received by all the slave supervisors. However, since the slave supervisor 1110 has been addressed, the distributed arbitrator and enable generator 1118 will generate an enable signal to an AND gate 1122. The AND gate 1122 receives the address bits on lines 1123 to generate the A0 through A13 address bits to a bus 1124 of the slave supervisor. Each slave supervisor is programmed to check to determine if the master supervisor is allotting hall calls. If the master supervisor 55 is allotting hall calls and the slave supervisor 1110 has been addressed, the distributed arbitrator and enable generator 1118 will have requested control of the bus 1124. When the slave processor is ready for some hall call data, the bus control is granted and the enable signal is generated to the AND gate 1122 to place the address bits on the bus 1124. The distributed arbitrator and enable generator 1118 will also generate a DIP signal to enable the address bits to be read by the slave processor.

Detailed Description Text (463):
Typically, a two car elevator system may include a first and a second car for serving at least two stations. Each car includes control means for instituting a change in the operation of its associated car in response to a plurality of control signals for that car. There is also for each car a source of signals characteristic of service conditions for that car and a supervisor with means for processing different ones of the service condition signals and generating a portion of each of the pluralities of control signals. The control means and the service condition signals source for each car are connected to the processing means for that car. A third source of service condition signals which are common to both cars is connected to the processing means for the second car where they are processed and the remainder of the first and secone pluralities of control signals are generated. The first and second processing means are connected so that the remainder of the first plurality of control signals can be transmitted to the first processing means. The third service condition signals may represent calls for service at the stations and the second processing means may allot the control signals generated from these service condition signals. Therefore, the first car is the slave and the second car is the master.

Detailed Description Text (464):
Data is also transmitted from the slave processors to the master processor. Position data for each elevator car is provided for use by the master processor in the allotment of hall calls. A slave supervisor will generate position data which is stored in the slave multi-car supervisor circuit. The slave multi-car supervisor circuit then sends the position data to the master multi-car supervisor circuit from which it is read by the master processor.

Detailed Description Text (466):
Thus, the elevator system according to the present invention utilizes a processor to perform all the logic and control functions for a single elevator car. Furthermore, in a multi-car system, a master processor also allots system hall calls to the other processors in the system while other control functions are handled on an individual basis. Although the present invention has been illustrated as an elevator system, it may be utilized to control a system having vehicles which selectively stop at stations along a predetermined path of travel such as mass transportation systems.

Detailed Description Paragraph Table (1):
221 4 line to 16 line decoder/demultiplexer 222 1 to 16 data selector/multiplexer 231 Bus interface circuit 235 Bus temporary memory 239 Transmitter receiver interface circuit 243 Transmitter and clock 246 Receiver 249 Failure detector A0 - A6, A8 Inverted address bits A0 - A13 Bus address bits BUSR Bus read signal BUSW Bus write signal CK Clock basic pulse train CK0, CK1, CK1, CK2, CK3, CK4 Clock output pulse trains DIP Bus data input signal DOP Bus data output signal DO Data for memory signal D0 - D5 Bus data bits E1 - E5 Data selector/multiplexer and decoder/demultiplexer enable signals EW Enable write signal L0, L1 - L5 Hall lantern address signals MSOK Master multiplexer failure signal MXDI Demultiplexed data in signals RA, RB Multiplexed data received RCV Receiver status signal RCV OUTPUT Transmitter status signal RDAT Data received signal SLOK Slave multiplexer failure signal STHL Generate hall lantern address signals signal W1 - W4 Data selector/multiplexer output signals XA, XB Multiplexed data transmitted XDAT Data signals to be transmitted XMT Enable transmitter signal

CLAIMS:

2. An elevator supervisor according to claim 1 wherein said bus means signal transmission lines include a plurality of address lines, data lines and control lines for transmitting information.

3. An elevator supervisor according to claim 1 wherein said processor includes memory means for storing velocity pattern data and means for generating velocity pattern control signals in response to said car position signals, said car velocity signals and said velocity pattern data and wherein said processing means transmits said velocity pattern control signals through said bus means and said position-velocity circuit to the elevator system control means for controlling the velocity of the elevator car.

6. An elevator supervisor according to claim 1 wherein said supervisor interface circuit generates information signals in response to said service condition signals and generates said control signals in response to processed information signals and wherein said processing means includes:

a bus interface means connected to said bus means signal transmission lines for transmitting said information signals and said processed information signals;

a first storage means for storing said information signals;

an arithmetic logic unit for performing a selected one of a plurality of arithmetic and logic functions on said information signals to generate said processed information signals and connected to receive said information signals from said first storage means;

a second storage means for storing said processed information signals and connected to receive said processed information signals from said arithmetic logic unit;

multiplexing means connected between said first storage means and said bus

interface means for controlling the flow of said information signals from said bus interface means to said first storage means and connected between said second storage means and said bus interface means for controlling the flow of said processed information signals from said second storage means to said bus interface means; and

control means for generating multiplexing means control signals to said multiplexing means to determine the sequence and timing of the flow of said information signals and said processed information signals.

12. An elevator system according to claim 10 wherein the other supervisors are designated as slave supervisors and including means connecting said master supervisor and said slave supervisors in parallel for transmitting said car stop signal from said master supervisor to a selected one of said slave supervisors.

34. A transportation system comprising:

a predetermined path of travel including at least two stations;

a first vehicle movable along said path of travel for serving said stations and including control means for instituting a change in operation of said vehicle in response to a first plurality of control signals;

a first source of signals characteristic of service conditions for said first vehicle;

a first supervisor for said first vehicle including a first means for processing a plurality of different ones of said first service condition signals and generating a portion of said first plurality of control signals and a first means connecting said first vehicle control means and said first service condition signals source to said first processing means;

a second vehicle movable along said path of travel for serving said stations and including control means for instituting a change in operation of said vehicle in response to a second plurality of control signals;

a second source of signals characteristic of service conditions for said second vehicle;

a second supervisor for said second vehicle including a second means for processing a plurality of different ones of said second service condition signals and generating a portion of said second plurality of control signals and a second means connecting said second vehicle control means and said second service condition signals source of said second processing means;

a third source of signals characteristic of service conditions which are common to said first and second vehicles connected to said second processing means by said second connecting means wherein said second processing means processes a plurality of different ones of said third service condition signals and generates the remainder of said first and second pluralities of control signals; and

a third means connecting said first processing means to said second processing means for transmitting the remainder of said first plurality of control signals to said first processing means.

35. A transportation system according to claim 34 wherein said third service conditions signals source includes means for issuing signals representing calls for service at said stations and wherein said second processing means processes said call signals individually and generates corresponding control signals to condition said first and second vehicles to service said calls.

36. A transportation system according to claim 35 wherein said second processing means allots individual ones of said call signals to said first or said second vehicles in accordance with their ability to serve the calls.

40. A transportation system according to claim 39 wherein said third service conditions signal source includes means for issuing signals representing calls for service at said stations, wherein said second connecting means includes an interface circuit connected between said signal issuing means and said bus and wherein said second processing means processes said call signals individually and generates corresponding ones of said remainder of said first and second pluralities of control signals to condition said first and second vehicles to service said calls.

49. A transportation system including a vehicle movable along a predetermined path of travel having at least two stations which the vehicle serves, control means for controlling the vehicle in response to control signals, a source of data signals characteristic of service conditions for the system and a supervisor for the vehicle responsive to the service conditions signals for generating the control signals, the supervisor comprising:

a bus means having a plurality of signal transmission lines;

at least one supervisor interface circuit connecting the service condition signal source and the control means to said bus means signal transmission lines; and

a processing means connected to said bus means for receiving said service condition signals and for generating said control signals in response thereto through said supervisor interface circuits, said processing means including:

a bus interface means connected to said bus means for controlling the admission of said service condition signals to and the transmission of said control signals from said processing means;

a first register means for storing one of said service condition signals;

an arithmetic logic unit for performing a selected one of a plurality of arithmetic and logic functions on an address signal and on said service condition signal to generate one of said control signals and connected to receive said service condition signal and said address signal from said first register means;

a second register means for storing said control signal and said address signal and connected to receive said control signal and said address signal from said arithmetic logic unit; multiplexing means connected between said first register means and said bus interface means for controlling the flow of said service condition signals from said bus interface means to said first register means, connected between said second register means and said bus interface means for controlling the flow of said control signals from said second register means to said bus interface means and connected between said second register means and said first register means for controlling the flow of said address signal from said second register means to said arithmetic logic unit;

memory means for storing a plurality of program instructions in a predetermined order and for generating a selected program instruction signal in response to said address signal; and

processor control means responsive to said program instruction signal for generating multiplexing means control signals to said multiplexing means to determine the sequence and timing of the flow of said service condition signals, said control signals and said address signal and for generating a function select

signal to said arithmetic logic unit to select the functions to be performed.

Refine Search

Search Results -

Term	Documents
(14 AND 17).PGPB,USPT,EPAB,JPAB,DWPI,TDBD.	4
(L14 AND L17).PGPB,USPT,EPAB,JPAB,DWPI,TDBD.	4

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
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Search History

DATE: Tuesday, February 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=ADJ			
L18	l14 and L17	4	L18
L17	l15 and L16	19940	L17
L16	frequency near2 pulse	95956	L16
L15	power near2 supply	633354	L15
L14	l12 and detect$3	135	L14
L13	l7 and L12	2	L13
L12	l5 and L11	150	L12
L11	l2 and L4	1370	L11
L10	L1 and l8	2	L10
L9	l2 and L8	2	L9
L8	l6 and L7	18	L8
L7	bus near2 manager	756	L7
L6	l4 and L5	6538	L6

h e b b cg b e e ch

L5	switch$2 near2 off	216610	L5
L4	data near2 communicat$3	161457	L4
L3	data near2 communicat$3 near2 switch$3 near2 off near2 state	0	L3
L2	network and L1	3384	L2
L1	vehicle near2 communication$1	10990	L1

END OF SEARCH HISTORY

h e b b cg b e e ch